

High-Speed 32-Bit Pattern and Handshaked Digital I/O

6533 Family (DIO 32HS)

6533 Family

PCI-DIO-32HS
PXI-6533
DAQCard-6533
AT-DIO-32HS

Digital I/O

32 (5V/TTL) digital I/O lines
Pattern I/O up to 13 Mbytes/s (PCI)
Handshaked I/O up to
76 Mbytes/s (PCI)
Two independent data paths
8, 16, or 32-bit transfers
Start and stop triggering
Pattern and change detection

NI-DAQ Software

Windows NT/98/95
Mac OS*
(refer to page 200 for other
operating systems)
*Not for all hardware

Application Software

LabVIEW
BridgeVIEW
LabWindows/CVI
Lookout
ComponentWorks
VirtualBench

Solutions

Automated test equipment (ATE)
Pattern recognition/generation
Electronic and logic testing
Board and chip verification
Digital comparison testing
Parallel digital communication
Interface to electromechanical and
solid-state relays
Interface to custom test equipment



Family	Digital I/O	Transfer Rate	Range	Handshaking	Pattern Generation	Triggers
6533	32	Up to 13 Mbytes/s (pattern I/O) Up to 76 Mbytes/s (handshaking)	5 V/TTL	✓	✓	✓

*Transfer rates shown are example rates for PCI version only. See product specifications on page 331 for more information. Pattern I/O rate is for gap-free transfer without wait states. Handshaking rate is for an ACK/REQ handshaking protocol allowing wait states.

Table 1. 6533 Family Specifications Overview (refer to page 331 for more detailed specifications)

Overview

The 6533 (DIO-32HS) is a high-speed, 32-bit, parallel digital I/O interface for PCI, PXI, CompactPCI, PCMCIA, and ISA computers. The 6533 incorporates the National Instruments DAQ-DIO ASIC, a 32-bit general-purpose digital I/O interface specifically designed to deliver high performance on plug-in digital I/O boards. The 6533 performs single-point I/O, pattern I/O, and high-speed data transfer using a wide range of handshaking protocols at speeds up to 76 Mbytes/s (PCI). You can operate the 32 lines as individually configurable single-line I/O, or as 8, 16, or 32-bit ports for pattern I/O and handshaking.

Hardware DAQ-DIO ASIC

The DAQ-DIO ASIC is a 32-bit general-purpose digital I/O interface that delivers advanced features to DIO boards at a low cost. These features include individually configurable I/O lines, wired-OR outputs, change detection, pattern detection triggering, high-speed handshaking protocols, and 16-word first-in-first-out (FIFO) buffers.

Data Latches and Drivers

The 32 digital I/O lines are divided into four 8-bit ports. The ports can be grouped into two 8-bit or 16-bit groups or a single 32-bit group for pattern I/O or handshaking. Each I/O line is 5 V/TTL-compatible. When configured for standard output, each data line can sink or source 24 mA when set logic low or high, respectively. When configured as inputs, the 6533 data lines are diode-terminated to dampen line reflections.

When not using handshaking or group operations, you can individually configure each of the 32 I/O lines as input or output. You can also choose standard or wired-OR outputs. Wired-OR outputs sink 24 mA when logic low, but do not source current when logic high. Unlike standard outputs, two or more wired-OR outputs can drive a single line.

Pattern I/O

Pattern I/O is reading (data acquisition) or writing (waveform generation) digital data at a predetermined rate without wait states. You control this rate internally by onboard counters or by an externally supplied frequency. The 6533 works with start and stop triggering as well as digital pattern detection. The stop trigger is the primary trigger. The 6533 transfers specified

High-Speed 32-Bit Pattern and Handshaked Digital I/O

6533 Family (DIO 32HS)

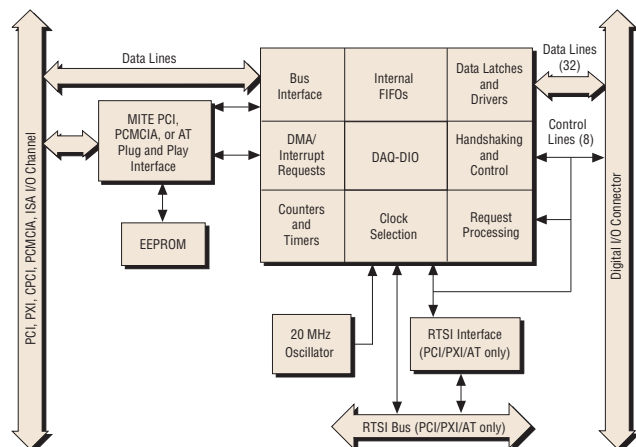


Figure 1. 6533 Family Hardware Block Diagram

amounts of data both before and after a stop trigger. If you do not enable a stop trigger, the 6533 stops automatically after transferring a number of data points equal to the size of your buffer.

The start trigger is a second trigger that begins a pattern generation operation. If you do not enable a start trigger, the operation starts immediately when you issue a software command to perform a transfer. These triggers are available for both digital data acquisition and digital waveform generation.

Pattern and Change Detection

In pattern detection mode, the 6533 triggers when a user defined input pattern occurs. In change detection mode, the 6533 monitors the input lines and captures data whenever there is a transition on one of the lines. In both pattern and change detection modes, you can specify a mask to indicate which data bits to examine.

Handshaking I/O

Handshaking I/O is similar to pattern I/O, except that data can speed up and slow down, instead of running at a predetermined rate. The handshaking process inserts wait states as needed. The 6533 and the peripheral device each provides the other with strobe signals as data becomes available or is acquired. By withholding strobe signals, either the 6533 or the peripheral device can slow down the transfer. When fixed rates are not critical, you can run handshaking operations to

obtain the highest possible speeds. The 6533 works with six different handshaking protocols. The protocol you select determines the timing of the Acknowledge (ACK) signals that the 6533 sends to the peripheral device and of the Request (REQ) signals expected from the peripheral device. You can customize each handshaking mode with programmable delays and polarities (See Table 2.)

8255 Emulation

This protocol emulates the strobed protocols implemented by the 8255 and 82C55 PPI chips – chips that are used on DIO-24 and DIO-96 devices. Because of faster response times, a wider data path, and use of FIFO buffering, 8255 emulation mode offers much higher data transfer rates than with an actual 8255 chip.

Level ACK

After each transfer, the 6533 asserts the ACK signal to the peripheral device. Holding the ACK line at the asserted level, the 6533 board does not begin a new transfer until a false-to-true transition on the REQ line from the peripheral device occurs.

Leading-Edge Pulse

After each transfer, the 6533 sends a pulse on the ACK line to the peripheral device. The 6533 then waits for a false-to-true transition on the REQ line, the start of a REQ pulse, before starting a new transfer. You can specify an ACK pulse delay.

Long Pulse

Long-pulse mode is the same as leading-edge pulse mode, except that you can specify a minimum pulse width, instead of an ACK pulse delay.

Trailing-Edge Pulse

After each transfer, the 6533 sends a pulse on the ACK line to the peripheral device. The 6533 waits for a true-to-false

Protocol	Peak Rates (Mwords/s) by Cable Length			REQ and ACK Polarity	REQ Edge-mode	Programmable Delay	Complementary Protocols
	1 m	2 m	5 m				
8255 Emulation Level ACK	6.67	4	4	Active-low	Trailing	Between transfers	Leading-Edge
	3.33	2.5	2.5	Programmable	Leading	Before ACK and between transfers	Level-ACK
Leading-Edge Pulse	3.33	2.5	2.5	Programmable	Leading	Before ACK and between transfers	Leading-Edge Pulse
Long Pulse	3.33	2.5	2.5	Programmable	Leading	For pulsewidth and between transfers, DIO-96, 8255, 82C55	Long Pulse, 8255-Emulation, DIO-24, DIO-96, 8255, 82C55
Trailing-Edge Pulse	1.8	1.5	1.5	Programmable	Trailing	For pulsewidth and between transfers	Trailing-Edge Pulse
Burst	20	10	10	Programmable	Neither; uses level REQ	For clock speed	Burst

Table 2. 6533 Family Handshaking Protocols

Data Acquisition

National Instruments

Phone: (512) 794-0100 • Fax: (512) 683-8411 • info@natinst.com • www.natinst.com

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transition on the REQ line, the end of a REQ pulse, before starting a new transfer.

Burst Mode

The 6533 sends or receives a clock signal to or from the peripheral device over an additional timing line (PCLK). The 6533 asserts an ACK signal if ready for a transfer, and the peripheral device, likewise, asserts a REQ signal if ready for a transfer. On each cycle of the PCLK that both the 6533 and the peripheral device are ready for a transfer, one data point is latched. In burst mode, data is transferred at high rates, particularly over short cables.

Table 2 shows similarities and differences among 6533 handshaking modes. It shows peak handshaking rates for typical cable lengths, the required polarity of the REQ and ACK signals, and complementary protocols with which each protocol can communicate.

Start-Up States

The 6533 has two lines on the I/O connector – CPULL and DPULL – with which you can select the biasing of the control and data signals, respectively. Connecting these lines to the onboard +5 V pulls the I/O and control lines high initially. Connecting these lines to GND or leaving them unconnected pulls the I/O and control lines low initially. Therefore, CPULL and DPULL lines control whether you get high or low control and data lines, when you power up the 6533 or reset its drivers.

DMA Control Circuitry

The PCI-DIO-32HS and PXI-6533 use the National Instruments MITE PCI interface. The MITE provides bus-master operation, PCI burst transfers, and high-performance DMA controllers for fast, continuous, scatter-gather DMA. Because the MITE contains its own DMA logic, the PCI-DIO-32HS and PXI-6533 require no DMA resources from your computer. The AT-DIO-32HS uses 16-bit, demand-mode DMA to maximize data transfer speed over the ISA bus. Onboard DMA circuitry packs or unpacks data from 16-bit DMA cycles to the I/O transfer sizes you select (8, 16, or 32-bits). The AT-DIO-32HS can also handle dual DMA, eliminating reprogramming delays by allocating both DMA channels to a single operation.

RTSI and PXI Trigger Interface

The 6533 uses the RTSI bus (PCI and AT) and the PXI trigger bus (PXI) to send timing signals to other boards for synchronization of simultaneous analog inputs, analog outputs, counters, digital inputs, and digital outputs. You can send the 6533 handshaking REQ, ACK, clock, and trigger lines across the RTSI and PXI Trigger buses. This feature is useful for synchronizing pattern I/O and handshaking with operations on other boards.

Digital I/O Connector

All digital I/O is through a 68-pin cable connector. See pin assignments in Figure 2. The 8-bit digital I/O ports are labeled DIOA, DIOB, DIOC, and DIOD, which are numbered ports 0, 1, 2, and 3, respectively. The dual sets of handshaking lines are REQ1 and ACK1, and REQ2 and ACK2. The trigger and clock lines are labeled STOPTRIG1 and PCLK1, and STOPTRIG2 and PCLK2. When the 6533 is not configured for group operations, the handshaking, triggering, and clock lines may be used as multipurpose I/O lines. The CPULL and DPULL lines determine the power-on state for the control lines and data lines, respectively. To use the 6533 (DIO-32HS) with 50-pin accessories or as a replacement for an AT-DIO-32F in a 50-pin application, use the 68F-50M DIO adapter (183139-02) with your existing cables and 50-pin digital accessories. See Table 3 for appropriate board and cable combinations.

DIO07	34	68	GND
GND	33	67	DIO06
DIO04	32	66	DIO05
DIO03	31	65	GND
GND	30	64	DIO02
DIO00	29	63	DIO01
DIO07	28	62	GND
GND	27	61	DIO06
DIO04	26	60	DIO05
DIO03	25	59	GND
GND	24	58	DIO02
DIO00	23	57	DIO01
DIO07	22	56	RGND
DIO06	21	55	GND
GND	20	54	DIO05
RGND	19	53	DIO04
GND	18	52	DIO03
DIO01	17	51	DIO02
DIO00	16	50	GND
DIOA7	15	49	GND
GND	14	48	DIOA6
DIOA4	13	47	DIOA5
DIOA3	12	46	GND
GND	11	45	DIOA2
DIOA0	10	44	DIOA1
REQ2	9	43	RGND
ACK2	8	42	GND
STOPTRIG2	7	41	GND
PCLK2	6	40	CPULL
PCLK1	5	39	GND
STOPTRIG1	4	38	DPULL
ACK1	3	37	GND
REQ1	2	36	GND
+5 V	1	35	RGND

Figure 2.
6533 Family
I/O Connector



For detailed product
specifications, refer to
page 331

Ordering Information

6533 Family

PCI-DIO-32HS for

Windows NT/98/95777314-01

Mac OS777314-02

PXI-6533777429-01

DAQCard-6533 for

Windows NT/98/95777315-01

Mac OS777315-02

AT-DIO-32HS777313-01

Includes NI-DAQ for Windows NT/98/95 on CD unless otherwise noted.

Example Configurations

Family	DAQ Board	Cable (page 305-309)	Accessory (page 295-304)
6533	PCI-DIO-32HS	SH68-68-D1 (183432-01)	SCB-68 (776844-01)
	PXI-6533	SH68-68-D1 (183432-01)	TBX-68 (777141-01)
	DAQCard-6533	PSHR68-68-D1 (777420-01)	SCB-68 (776844-01)
	AT-DIO-32HS	SH68-68-D1 (183432-01)	SCB-68 (776844-01)

Refer to page 205 for more detailed cable and accessory options.

Specifications

High-Speed Digital I/O (6533 Family)

These specifications are typical for 25 °C unless otherwise noted.

Digital I/O

Number of channels 32 input/output
4 dedicated output and control
4 dedicated input and status

Compatibility 5V/TTL
Hysteresis 500 mV

Digital Logic Levels

Level	Minimum	Maximum
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Output low voltage ($I_{out} = 24$ mA)	—	0.4 V
Output high voltage* ($I_{out} = 24$ mA)	2.4 V	—

*When configured as standard outputs. Drivers configured as wired-OR outputs are tri-stated when logic is high.

Maximum Input Voltage -0.3 to 5 V
Power-on state for outputs Tristated, pulled up or down (selectable)
Data transfers DMA, programmed I/O, interrupts

Pattern I/O

Direction Input or output
Modes Internally or externally timed, change detection

Transfer rate (maximum sustainable) System dependent¹

Transfer Rates in Mwords/s (Mbytes/s) on Sample Systems

Mode	Triton I Chip Set	Triton II Chip Set	Natoma Chip Set
PCI-DIO-32HS	Transfer Rates in Mwords/s (Mbytes/s) on Sample Systems		
Input	32-bit	2.8 (11.2)	4 (16)
	16-bit	4 (8)	5 (10)
	8-bit	6.67 (6.67)	10 (10)
Output	32-bit	1 (4)	2 (8)
	16-bit	1 (2)	2.5 (5)
	8-bit	2 (2)	5 (5)
PXI-6533	Transfer Rates in Mwords/s (Mbytes/s) on Sample Systems		
Input	32-bit	4 (16)	—
	16-bit	5 (10)	—
	8-bit	6.67 (6.67)	—
Output	32-bit	2.22 (8.88)	—
	16-bit	2.5 (5)	—
	8-bit	5 (5)	—
DAQCard-6533	Transfer Rates in Mwords/s (Mbytes/s) on Sample Systems		
32-bit	0.03 (0.12)	0.07 (0.28)	0.14 (0.56)
16-bit	0.035 (0.07)	0.075 (0.15)	0.165 (0.33)
8-bit	0.035 (0.035)	0.075 (0.075)	0.165 (0.165)
AT-DIO-32HS	Transfer Rates in Mwords/s (Mbytes/s) on Sample Systems		
32-bit	0.35 (1.4)	—	—
16-bit	0.7 (1.4)	—	—
8-bit	1.4 (1.4)	—	—

Handshaking

Direction Input or output
Modes 6 (burst, level-ACK, leading-edge pulse, trailing-edge pulse, long pulse, and 8255 emulation)

Transfer Rate² (maximum)

Board	Width	Maximum Transfer Rate	
		Mwords/s	Mbytes/s
PCI-DIO-32HS	32-bit	19	76
	16-bit	19	38
	8-bit	19	19
PXI-6533	32-bit	16	64
	16-bit	17	34
	8-bit	19	19
DAQCard-6533	32-bit	0.185	0.740
	16-bit	0.235	0.470
	8-bit	0.235	0.235
AT-DIO-32HS	32-bit	0.45	1.8
	16-bit	0.9	1.8
	8-bit	1.8	1.8

Start and Stop Triggers

Compatibility 5V/TTL
Trigger types Rising or falling edge, digital pattern
Pulsewidth for edge triggers 10 ns, minimum
Pattern triggers detection capabilities Detect pattern match or mismatch on user-selected bits

RTSI Triggers (PCI and AT Only)

Trigger lines 7

PXI Trigger Bus

Trigger lines 7

Bus Interfaces

PCI, PXI Master, slave
DAQCard PCMCIA slave
AT AT slave with dual DMA

Power Requirement

+5 VDC (±5%) 500 mA typical (with light output load)
Power Available at I/O connector

PCI, PXI, AT +4.65 to +5.25 VDC, 1 A
DAQCard +4.65 to +5.25 VDC, 250 mA

Physical

Dimensions, not including connectors

PCI, AT 17.5 by 10.7 cm (6.9 by 4.2 in.)
PXI 10 by 16 cm (3.9 by 6.3 in.)
DAQCard Type II PC Card

I/O Connector

PCI, PXI, AT 68-pin male SCSIII type
DAQCard 68-pin female PCMCIA

Environment

Operating temperature 0 to 55 °C, DAQCard should not exceed 55 °C while in PCMCIA slot
Storage temperature -20 to 70 °C
Relative humidity 10% to 90% noncondensing

Specifications

Static Digital I/O (continued)

PXI-6508.....	10 by 16 cm (3.9 by 6.3 in.)
PC-DIO-96.....	16.5 by 9.9 cm (6.3 by 3.9 in.)
DAQPad-6507/8.....	14.6 by 21.3 by 3.8 cm (5.8 by 8.4 by 1.5 in.)
I/O connector	
6503, except DAQCard.....	50-pin male
DAQCard-DIO-24.....	25-pin female PCMCIA
6507/8, except PC-DIO-96.....	100-pin female 0.050 series D-type
PC-DIO-96.....	100-pin male ribbon cable

Environment

Operating temperature.....	0 to 55 °C, DAQCard should not exceed 55 °C while in PCMCIA slot
Storage temperature.....	-20 to 70 °C
Relative humidity.....	10% to 90% noncondensing

For information on static digital I/O in the VXI form factor refer to the VXI Catalogue.

Optically Isolated Digital I/O (OPDIO) I/O Electrical Specifications

Compatibility.....	5V/TTL
Configuration.....	Optically isolated digital channels 8 dedicated input, 8 dedicated output

Digital Input

Number of channels.....	8, each with its own ground reference isolated from other channels
Maximum input voltage.....	24 VDC or 24 VAC

Digital Logic Levels

Level	Minimum	Maximum
Input low voltage (DC or peak AC)	–	±1 V
Input high voltage DC 1 kHz AC	±2 VDC 4 V _{rms}	±24 VDC 24 VAC

Input current	
5 V inputs.....	1.5 mA/channel
24 V inputs.....	7.0 mA/channel
Isolation.....	24 V from computer ground

Digital Output

Number of channels.....	8, each with its own common reference and supply pins isolated from other channels
External voltage supply.....	5 to 24 VDC

Digital Logic Levels

Level	Minimum	Maximum
Output low voltage ($I_{out} = 4$ mA)	–	±1 VDC
Output high voltage ($I_{out} = 250$ μ A) VCC0=24 V VCC0=5 V	22 VDC 3 VDC	– –
Output low current	–	7.0 mA

Supply Current for isolated outputs

5 V outputs.....	5 mA/channel min
24 V outputs.....	10 mA/channel min
Isolation.....	24 V from computer ground

Power Requirements

+5 VDC (±5%).....	500 mA max
Power Available at I/O connector.....	+5 VDC, 1 A

Physical

Dimensions.....	10.8 by 12.1 cm (4.3 by 4.8 in.)
I/O connector.....	50-pin male

Environment

Operating temperature.....	0 to 50 °C
Storage temperature.....	-20 to 70 °C
Relative humidity.....	10% to 90% noncondensing

Low-Cost Electromechanical Relays (ER-8/16)

Digital Relays

Number of relays.....	8 relays for ER-8 16 relays for ER-16
Relay type.....	SPDT (Form C), nonlatching
Maximum switching capacity (resistive load)	
AC.....	3 A at 250 VAC
DC.....	3 A at 30 VDC
Maximum working voltage.....	250 Vrms (relay to ground) 250 Vrms (relay to relay – same phase)
Switching current	
Per relay.....	3 A max
All relays.....	24 A max for ER-8 40 A max for ER-16
On resistance.....	100 m Ω
Contact material.....	Silver-nickel alloy
Expected life	
Mechanical.....	10,000,000 operations, minimum
Electrical.....	100,000 at maximum rated load
Isolation, coil to contacts.....	2,000 Vrms
Relay operate time.....	10 ms
Relay release time.....	5 ms

Power Requirements

+5 V (±5%).....	0.5 A per group of 8 relays
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Physical

Dimensions.....	17.5 by 5.2 by 12.3 cm (6.9 by 2.1 by 4.8 in.)
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Connectors

External.....	50-pin male
Internal.....	26-pin male
Relay screw terminals.....	24 for ER-8, 16 AWG wire max 48 for ER-16, 18 AWG wire max

Power Supply screw terminals.....	2
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Environment

Operating temperature.....	0 to 50 °C
Storage temperature.....	-20 to 70 °C
Relative humidity.....	10% to 90% noncondensing

¹ Pattern generation rates depend on your computer, software, and other bus activity. The rates shown were measured for 100 Ksample transfers on sample Intel Pentium-based computers, using NI-DAQ software, with no other DAQ operations in progress. The PCI Triton I rates were measured on a 100 MHz Pentium computer with the Triton I (430FX) chip set. The PCI Triton II rates were measured on a 166 MHz Pentium computer with the Triton II HX (430HX) chip set. The PCI Natoma rates were measured on a 180 MHz Pentium Pro system with the Natoma (440FX) chip set. The PXI Triton I rates were measured on a 133 MHz CompactPCI Pentium computer with the Triton I (430FX) chip set. The ATDIO-32HS rates were measured using the dual-DMA transfer method on a 100 MHz Pentium computer with the Triton II (430FX) chip set. The DAQCard Triton I rates were measured using a 75 MHz Pentium computer with the Triton I (430FX) chip set. The DAQCard Triton II rates were measured using a 133 MHz Pentium computer with the Triton II (430HX) chip set. The DAQCard Natoma rates were measured using a 266 MHz Pentium II computer with the Natoma (440FX) chip set.

² Handshaking rates depend on your computer, software, other bus activity, and handshaking protocol. The rates shown were measured using NI-DAQ software and the burst-mode handshaking protocol, performing continuous waveform generation using 100,000-point or larger buffers, with no other DAQ operations in progress. The AT-DIO-32HS, PCI-DIO-32HS, and PXI-6533 handshaking rates are DMA-based and do not necessarily increase as the speed of the computer increases. The AT-DIO-32HS and PC-DIO-32HS rates shown were measured on a sample 100 MHz Intel Pentium-based computer with an Intel 430FX (Triton I) chip set. The PXI-6533 rates shown were measured on a sample 133 MHz Intel Pentium-based CompactPCI computer with an Intel 430FX (Triton II) chip set. The DAQCard-6533 rates do tend to increase as the speed of the computer increases. The DAQCard rates were measured using a 266 MHz Pentium II computer with the Natoma (440FX) chip set.

³ Transfer rate depends on the computer and software. The rates may vary due to programming language and code efficiency, CPU utilization, transfer methods, and so on. Please consult the user manual for specifics. The DAQPad-650x transfer rate is dependent upon available USB bandwidth. Expect much slower rates.

National Instruments

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