

WATERS CORPORATION

PERFORMANCE SPECIFICATION

TYPE OF SPECIFICATION (check one):

☐

SYSTEM

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SUB ASSEMBLY

PRODUCT: H-Class Products

DOCUMENT NUMBER: 810000520

ASSEMBLY NAME: 3VCCPU AHCT

REVISION: B

PART NUMBER AFFECTED: 210000520

WRITTEN BY: Gary Fragoza

UPDATED By: Ziad El-Massih

DATE: 02/08/2011

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INTRODUCTION

1.1. DOCUMENT INTENT

The intent of this document is to provide reader with a detailed hardware description and performance specification for the 3VCCPU PCB design. The intended audience is Software Development, Test Engineering, Hardware Engineers etc. The three perspectives considered are performance to the customer, testing of the assembly and future applications of the assembly. Document information will include critical function theory of operation, software control instructions, hardware register definitions, memory map information and I/O electrical specifications. The intent of this document is to provide the reader with additional information not contained in the associated documentation listed in Section 1.3 titled "REFERENCE DOCUMENTATION".

1.2. PRODUCT DESCRIPTION

This new CPU version P/N 210000520 is identical to 3VCCPU, P/N 210000273, except for the following Changes:

Rev A Changes:

- The signals translators used to download the FPGA image onto the Personality PCB, U13, U20, and U21 were changed from LVC family to AHCT family. In addition, R159 was changed from 51 OHM to Zero OHM. These changes were needed to slow down the signal edges which can help preventing image download failures in some older products.
- A pull-up resistor was added to the RS-232 Transmit input T1IN and a pull-down resistor to unused T2IN. The pull-up resistor was needed to have the RS-232 chip's output to be in a known state when the system is still in reset during power up. This fix will solve the communication problem found when Rheodyne LabPro is connected to Waters instruments.
- The board layout is identical to the 210000273 except for adding very short traces to the added RS-232 resistors.

Rev B Changes:

- The obsolete NVRAM controller (332000367, ST Microelectronics M40SZ100W) was replaced with a functionally equivalent part (332000834, Maxim, DS1314S-2+).
- All the Rev A changes were carried forward to Rev B.

The 3VCCPU PCB may be broken down into the following major functional sections required to perform the following major functions: the Microprocessor, SRAM, NVRAM, Flash Memory functions, RS232, Ethernet functions, QSPI Serial Interface, Time Processing Unit and Miscellaneous Memory Mapped I/O Functions (i.e. interrupts, Chip Selects, etc). Also included is an In Circuit Emulator (ICE) interface required for software design and software/hardware integration.

1.3. REFERENCE DOCUMENTATION

The following table describes the reference material needed with this document.

WATERS PART NUMBER	DOCUMENTATION DESCRIPTION
210000520	ASSY, PCB, 3VCCPU AHCT
710000520	SCHEMATIC, PCB, 3VCCPU AHCT
510000520	PCB, 3VCCPU AHCT
610000520	A/W, PCB, 3VCCPU AHCT
361000366	Programmed, CPLD, 3V CPU2000
735002031	Common HW Register Addresses & Structures
Freescale MC68332 Homepage	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC68332&fsrch=1
Waters Intranet Site	Other IC Specifications as Required

Table 1 Reference Documents

1.4. SPECIFICATIONS

Most of the 3VCCPU physical dimensions can be found on the PCB Fabrication Drawing.

PCB Weight 75 Grams

Power Consumption 410 ma at 5VDC Max, (plus additional Overlay Memory at 150ma)

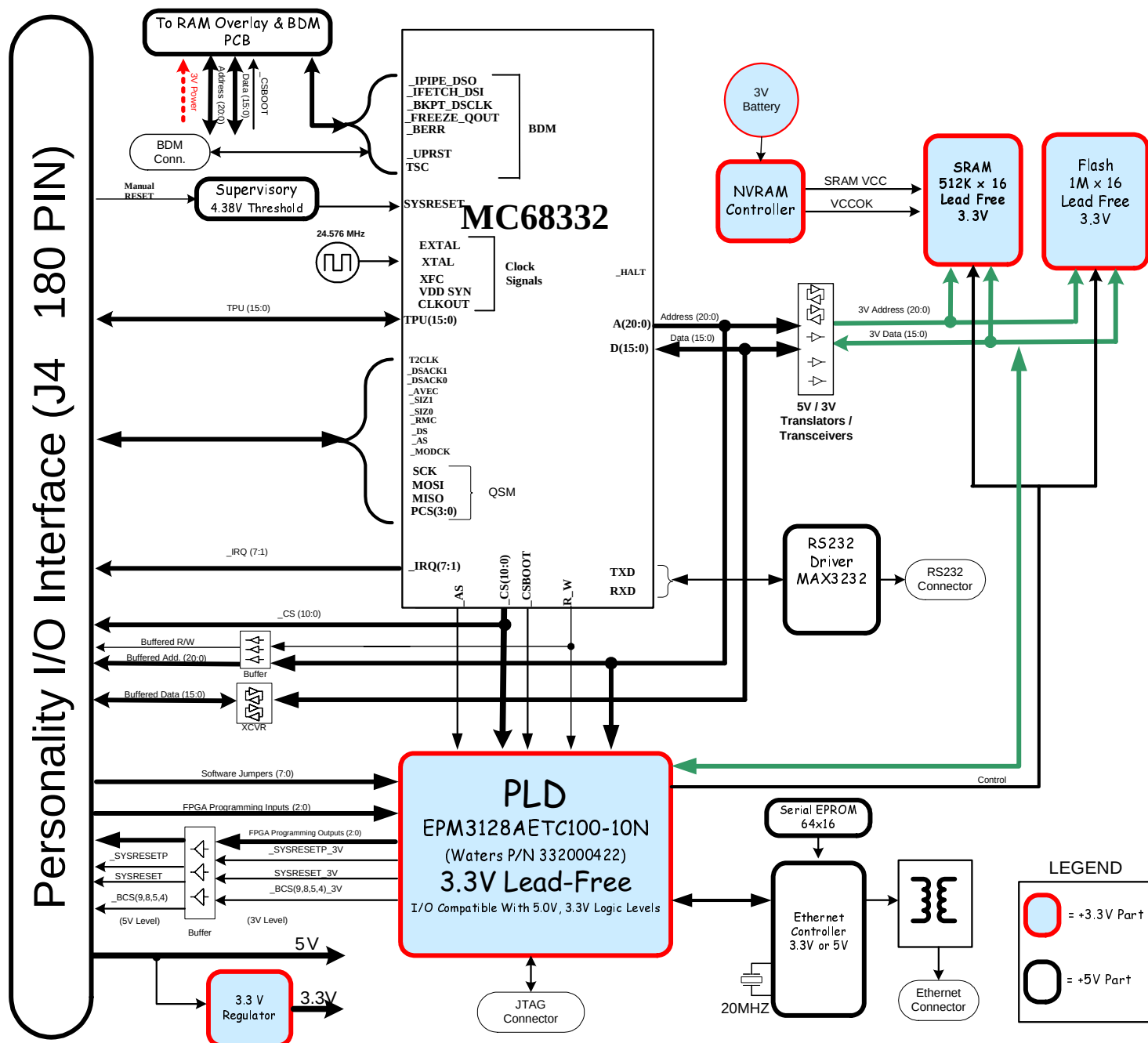
1.5. ENVIRONMENTAL SPECIFICATIONS

Operating temperature range	4 to 40 degrees C
Relative Humidity	20 % to 80 % (non-condensing)
Storage Temperature Range	-20 to 80 degrees C
Air Flow over PCB	None Required

1.6. SAFETY

The only voltage supplied to the 3VCCPU PCB is +5VDC, which is supplied through the 180-pin J4 connector. This is an intrinsically safe voltage so there are no safety concerns.

1.7. FUNCTIONAL BLOCK DIAGRAM



2. FUNCTIONAL DESIGN AND PERFORMANCE SPECIFICATIONS

2.1. 3VCCPU MEMORY MAP

Name	Base (Hex)	Size (Bytes)	Mode	Byte	R/W	Strobe	Dsack	Space	IPL	AVEC	Access Size	Function
CSBOOT**	000000	1M	Async	Both	Both	/AS**	0 Wait	S/U	All	OFF	16 bit	Flash0
CS0**	100000	1M	Async	Both	Both	/AS**	0 Wait	S/U	All	OFF	16 bit	Flash1 (for expansion)
CS1	200000	512k	Async	Lower	Both	/DS	1 Wait	S/U	All	OFF	16 bit	SRAM0
CS2	200000	512k	Async	Upper	Both	/DS	1 Wait	S/U	All	OFF	16 bit	SRAM1
CS3	300000	64k	Async	Both	Both	/DS	1 Wait	S/U	All	OFF	16 bit	Ethernet,_IRQ2
CS4*	400000	64k	Async	Both	Both	/AS	6 Wait	S/U	All	OFF	8 bit	LCD
CS5*	500000	64k	Async	Both	Both	/AS	2 Wait	S/U	All	OFF	8 bit	FPGA
CS6	FFF800	2K	Async	Both	Both	/AS	F Term	CPU	All	ON	ADDR	Used as Autovector (IACK, Also Address 19
CS7	FFF800	2K	Async	OFF	RSVD	/AS	F Term	CPU	All	OFF	ADDR	Address 20 For Flash Memory
CS8*	800000	64K	Async	Both	Both	/AS	5 Wait	S/U	All	OFF	8 bit	IEEE (8bytes Used)
CS9*	900000	64k	Async	Both	Both	/AS	1 Wait	S/U	All	OFF	16 bit	Unused by 3VCCPU
CS10	A00000	1M	Async	Both	Both	/AS	1 Wait	S/U	All	OFF	16 bit	FPGA Program port / ID port (4 words Used by 3VCCPU)

Table 2 Example of Typical EMULATOR SETUP for 3VCCPU 2000 (Settings used by BOOTLOADER also)

- ***Note:** CS4, 5, 8, 9 can be used for miscellaneous functions. Default usage is in Function column, i.e. CS4 as LCD interface, CS5 as FPGA interface etc.
- ****Note:** CSBOOT and CS0 must be strobed with /AS in order for the logic in the CPLD to correct a possible holdtime violation found in the original 5V CPU2000 when writing to Flash. The Boot Loader application for the 3V CPU 2000 has been modified to use /AS for the Flash address space.
- **CS6 is NOT used:** pin is used as A19, internally CS6 registers are set for Autovector function by BOOTLOADER (default use).
- **CS7 is set by BOOTLOADER to NOT be used selecting A20 pin functionality (default).**
Since A20 is NOT (and CAN NOT) be used, CS7 functionality can be restored, and pin/line called A20 can be used as CS7.
- **CS8 is used/reserved for IEEE488 interface by BOOTLOADER.** Firmware can change its function.
- **CS10 is used for the FPGA Programming port and for CPU & Personality IDs and Versions (part of address space used) as well as access to registers internal to CPLD on the 3VCCPU..**

2.2. 3VCCPU REGISTER DEFINITIONS

The obligatory values in the MC68332 CSx Registers above are based on the 25.17MHz processor timing listed in the datasheet.

2.2.1. MC68332 Registers

See MC68332 Users Manual Appendix D. for a detailed description of the registers internal to the MC68332 as initialized by the SIM Register File example in Section 3.3 of this document.

2.2.2. LOCAL 3VCCPU REGISTERS

Address is specified by denoting chip select and an address offset. Addresses are in hexadecimal notation.

The Base address is created by selecting a base address field, bits (15:3) in the Chip-Select Base Address Register, **CSBAR10**. CS10 base address is set by BOOTLOADER (default) to A00000.

For example, **Software Jumper Register** in the 3VCCPU is a memory mapped register at AC0002 as set by boot loader. It is CS10 relative (CS10 set for a base address of A00000) + offset of 0C0002.

Offset:	0x0C0000 -BYTE Access ONLY (Read Only)		
Name:	Peripheral ID REGISTER		
Initial Value:	Determined by Peripheral PCB		
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	Peripheral_ID7	0/1	Upper Byte = Peripheral ID
6	Peripheral_ID6	0/1	“
5	Peripheral_ID5	0/1	“
4	Peripheral_ID4	0/1	“
3	Peripheral_ID3	0/1	“
2	Peripheral_ID2	0/1	“
1	Peripheral_ID1	0/1	“
0	Peripheral_ID0	0/1	“

Offset:	0x0C0001 -BYTE Access ONLY (Read Only)		
Name:	CPU ID REGISTER		
Initial Value:	Determined by 3VCCPU – set to 02 for the current release		
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	3VCCPU_ID7	0	CPU ID
6	3VCCPU_ID6	0	“
5	3VCCPU_ID5	0	“
4	3VCCPU_ID4	0	“
3	3VCCPU_ID3	0	“
2	3VCCPU_ID2	0	“
1	3VCCPU_ID1	1	“
0	3VCCPU_ID0	0	“

Offset:	0x0C0002 WORD Access ONLY (Read Only)		
Name:	Software Jumper Register		
Initial Value:	xxxx		
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15		X	Upper Byte = Not Used
14		X	“
13		X	“
12		X	“
11		X	“
10		X	“
9		X	“
8		X	“
7	SFTWRJMPR7	1/0	Lower Byte =Jumpers (0 when ON)
6	SFTWRJMPR6	1/0	“
5	SFTWRJMPR5	1/0	“
4	SFTWRJMPR4	1/0	“
3	SFTWRJMPR3	1/0	“
2	SFTWRJMPR2	1/0	“
1	SFTWRJMPR1	1/0	“
0	SFTWRJMPR0	1/0	“

Offset:	0x0C0004 -WORD Access ONLY (Read/Write)		
Name:	FPGA Program Port		
Initial Value:	xxxx		
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15		X	
14		X	
13		X	
12		X	
11		X	
10		X	
9		X	
8		X	
7		X	
6		X	
5		X	
4	Prog. Output HiZ_1	0/1	See Truth Table 3 Below
3	Prog. Output HiZ_0	0/1	See Truth Table 3 Below
2	Program Port 2	0/1	Read = PNSTATUS, Write = PNCONFIG
1	Program Port 1	0/1	Read = PINIT_DONE, Write = PDCLK
0	Program Port 0	0/1	Read = PCONFIG_DONE, Write = PDATA

Prog. Output HiZ_1	Prog. Output HiZ_0	CONFIG_OE Output State (see section 2.5.3.7)	Config. Output Status
0	0	0	Config. outputs HiZ
0	1	1	Config. outputs driven
1	0	1	Config. outputs driven
1	1	1	Config. outputs driven

Table 3 FPGA Configuration Pin Tristate Truth Table

Offset:	0x0C0006 –WORD Access ONLY (Write Only)		
Name:	Ethernet Reset Port		
Initial Value:	xxxx		
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15		X	
14		X	
13		X	
12		X	
11		X	
10		X	
9		X	
8		X	
7		X	
6		X	
5		X	
4		X	
3		X	
2		X	
1		X	
0	Ethernet_RESET	0/1	1=Reset

2.2.3. Ethernet Controller Memory Map

Table of registers used and offsets are located within the LAN91C96 Users Manual accessible from the SMSC web site, <http://www.smsc.com/main/datasheets>, the Adobe Portable Document Format (PDF) file is: 91c96.pdf

2.3. 3VCCPU CORE

The 3VCCPU Core is based on a 32-bit integrated microcontroller, the MC68332. The MC68332 is configured to run at **24.576 MHz** in this design by an external oscillator Y2. The MC68332 also includes intelligent peripheral modules:

- Time Processor Unit (TPU) ,
- Queued Serial Module (QSM),
- System Integration Module (SIM).
- a 2K-byte standby/TPU emulator RAM

The 2K-Byte RAM (internal to MC68332) is not presently used as standby RAM but is used as emulator RAM for the TPU module.

2.4. 3VCCPU MC68332 INTERFACES

2.4.1. CPU32

The core of the MC68332, is a 32 bit CPU, called the CPU32. The CPU32 is upward code compatible with the MC68010 and also includes many MC68020 enhancements. The CPU 32 is based on a complex instruction set controller. Features of the CPU32 include:

- Upward Object Code Compatible
- New Instructions for Controller Applications
- 32-Bit Architecture
- Virtual Memory Implementation
- Loop Mode of Instruction Execution
- Table Lookup and Interpolate Instruction
- Improved Exception Handling for Controller Applications
- Trace on Change of Flow
- Hardware Breakpoint Signal, Background

Reference: See MC68332 User's Manual at link below, for more details.

http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC68332&fsrch=1

2.4.2. CPU Background Debug Interface

The 3V CPU 2000 supports 2 methods for background debug.

Method 1:

- P1 connector of 3VCCPU can be populated with a dual row 80-pin connector.
- A 2Mbyte RAM Overlay, PN 210000153, can be installed.
- The RAM Overlay also contains the 10-pin header to which the BDM signals from the MC68332 are connected. A VisionProbe style emulator can be plugged into the BDM Port.
 - A jumper between pins 1 and 2 of J1 (on the RAM Overlay board) enables the overlay SRAM and disables the Flash on the 3VCCPU.
 - The jumper must be removed to enable the Flash memory control interface which allows the Flash to be programmed through the BDM interface using (eg) the WindRiver Vision Click Software.

Method 2:

- J3 on the 3V CPU is an on-board 10-pin header to which the BDM signals from the MC68332 are connected. A VisionProbe style emulator can be plugged into this BDM Port.

2.4.3. Time Processor Unit

The TPU consists of a dedicated execution unit, a prioritized scheduler, data storage RAM, dual-time bases, and a microcode ROM. The TPU controls 16 independent, orthogonal channels capable of performing any time function. The 16 independent channels also contain a dedicated event register to allow both match and input capture functions. The algorithms available in microcoded ROM include:

- Discreet I/O
- Period Measurement with missing transition detection
- Period Measurement with additional transition detection
- Position-Synchronized Pulse Generator
- Stepper motor control
- Output Match
- Period/Pulse Width Accumulator
- synchronize channels to either of two 16-bit counters (w/pre-scaler)

The 16 channels plus the TCR2CLK are physically connected to the **3VCCPU** I/O connectors without buffers, since the TPU channels can be either input or output. The TPU signals are routed directly from the MC68332 to the **3VCCPU** I/O connector.

Reference: See TPU User's Manual for additional details.

2.4.4. Queued Serial Module

The QSM consists of two communication interfaces:

- Queued Serial Peripheral Interface (QSPI)

The QSPI provides easy peripheral expansion or inter-processor communication through a full-duplex, synchronous, three-line bus. Four programmable peripheral chip selects can select up to 16 peripheral devices. A self-contained RAM queue allows up to sixteen serial transfers of eight to sixteen bits each or transmission of a 256-bit data stream without CPU intervention. A special wraparound mode supports continuous sampling of a serial peripheral, with automatic QSPI RAM updating, for efficient inter-facing to A/D converters. The QSPI signals are routed to the 3VCCPU 180 pin I/O connector, J4.

- Serial Communications Interface (SCI)

The SCI is the Serial Communications Interface, portion of the Queued Serial Module (QSM) located within the MC68332. The SCI is utilized as a terminal port for software development purposes. There is no hardware handshaking implemented with the SCI port, and XON/XOFF can be used for flow control. The Serial Port consists of the M68332 SCI port and a MAX232 driver chip. The outputs of the MAX232 driver are connected through a surface mounted multi-layer ferrite bead to I/O Connector, J1.

2.4.5. System Integration Module

The SIM includes an external interface and various functions that reduce the need for external glue logic. Features of the SIM include:

- External Bus Support
- Programmable Chip-Select (CSx) Outputs (12 chip selects)
- System Protection Logic
- Watchdog Timer, Clock Monitor, and Bus Monitor
- Test/Debug Sub-module for Factory/User Test and Development

See the Memory Map in Table 2 for Chip select functional mapping.

Chip selects _CS4, _CS5, _CS8, and _CS9, are routed to the local CPLD where they are buffered then level translated to 5V CMOS levels (for legacy personality cards) before being driven onto the 180 pin I/O Connector, J4. The _CS10 chip select is driven onto the 180 pin I/O Connector J4 directly from the MC68332, however it also goes to the CPLD where it is internally decoded along with address lines to create the _IDENBIT control signal on the 180 pin I/O Connector J4.

2.5. 3VCCPU LOCAL INTERFACES

2.5.1. Memory Functions

The Memory Function consists of FLASH, SRAM and SRAM Overlay Control.

2.5.1.1. Flash

The Flash memory consists of one 1Mx16 Flash Memory device. The Flash is Byte or Word accessible and is organized into two logical banks where each is 512Kx16. Refer to Table 2 and Figure Figure 6 for chip select information and detailed settings. Bank0 is selected at Power-up reset by the CSBOOT chip select from the MC68332 MCU. All FLASH device memory will be allocated sequentially. The Flash memory control is located within the CPLD located on this 3VCCPU PCB.

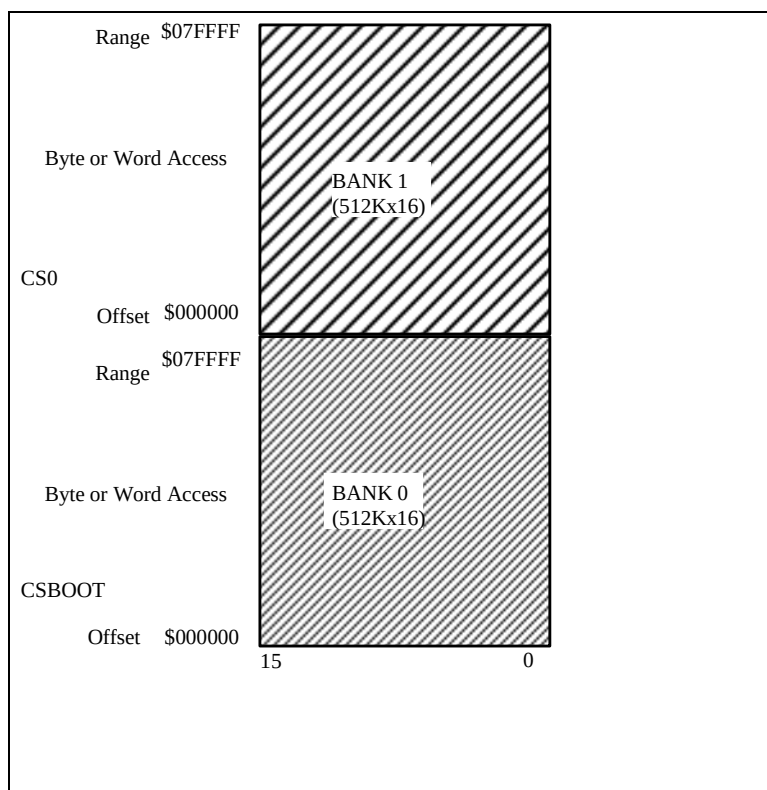


Figure 2- Flash Architecture

2.5.1.2. SRAM

There is 1MB of SRAM organized in a single 512Kx16 device. The single SRAM device is configured in two logical banks of 512Kx8 for byte access or a single logical bank of 512Kx16 for word access. For word access, both CS1 and CS2 go active at the same time. The entire 512Kx16 SRAM device is battery backed. See Figure 8.

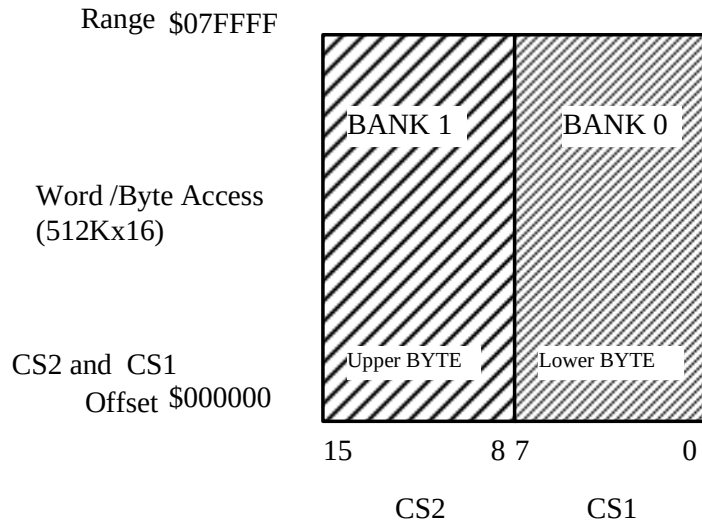


Figure 3- SRAM Architecture

The NVRAM controller (332000834, Maxim, DS1314S-2+) and the 3V Lithium Battery, provide the data retention for the SRAM. The NVRAM controller also write-protects the SRAM as VCC degrades during a power failure. When the 3V CPU is powered down, the NVRAM controller switches in the battery voltage to the SRAM to protect the contents. The battery capacity consumption is simply calculated by:

$$\text{BatteryCapacity} / [8760 \times (1 - (\text{VccDutyCycl}) / 100)) \times I_{\text{bat}}]$$

where:

- BatteryCapacity is measured in ampere-hours
- 8760 is the constant for the number of hours there are in a year
- VccDutyCycle is measured as a percentage
- I_{bat} is measured in amperes.

SRAM	Batt. Capacity (A-H)	SRAM Data Retention Curr. (Amps)	Max. I _{bat} (Amps) *Includes leakage from NVRAM controller	Battery Consumption (Min. Yrs.)
ISSI SRAM IS62WV25616BLL-55TLI	0.22	20x10 ⁻⁰⁶	20.1x10 ⁻⁰⁶	1.78

Table 4- Battery Life

VccDutyCycle = 33% (8hrs on time out of 24hrs)

BatteryCapacity=0.220 Ah (220mAh)

Note: *ST Microelectronics Application Note 1012 used as reference for Battery Life calculations.*

2.5.1.3. SRAM OVERLAY

The SRAM Overlay Control will allow replacement of Bank 0 and Bank 1 FLASH memory with SRAM for software debugging during the product development phase. This is done without sacrificing the hard real-time functions of the instruments during testing and debugging. The SRAM Overlay is configured as contiguous memory using the _CSBOOT and _CS0 chip selects. The SRAM Overlay is accessible in word or byte mode.

2.5.2. Local & Peripheral Bus Control

The Local and Peripheral Bus Control is accomplished within the CPLD U25 on 3VCCPU. The CPLD contains the glue logic necessary for controlling bus access to and from the MC68332 processor and memory and/or the peripheral bus. See CPLD VHDL code for details.

2.5.3. Peripheral Interface

The peripheral interface consists of the Address Bus, Data Bus, Chip Selects, TPU Port, QSPI Port, Ports E and F, FPGA Programming Port, CPU/Peripheral ID Interface

2.5.3.1. Address Bus

The address bus from the microprocessor, ADDR (20:0) is buffered through AHC245 drivers to the I/O Connector. The buffer is always enabled through the PADDR_OE signal output by the CPLD. ADDR19 and ADDR20 are intentionally swapped at the input to AHC245 buffer U4 to stay consistent with a design error made on the original 5V CPU2000.

2.5.3.2. Data Bus

The data bus from the microprocessor, DATA (15:0) is buffered through AHCT245 transceiver to the I/O Connector. The transceiver direction is controlled by the PR_W control signal which is the MC68332's R_W signal buffered through an AHC245 buffer.

2.5.3.3. Chip Selects

The following table details the max time to access a peripheral I/O and maintain the required WS. Additional WS should be added if a longer access time is required. Example : If CS5 is connected to a peripheral who's access time is 60ns then in the chip select option Register (CSOR) 5 the DSACK wait state insertion parameter should be equal to 1 for a total access time of 25ns + 40ns = 65ns, where 40ns is 1 wait state. (Data hold time on reads is 0ns.)

CS	Wait State	Peripheral Access Time Required (max in ns)	Comments	CSx Usage Local Peripheral
BT,0	0	90	Flash of 90 ns or faster required	L
1,2	1	70	SRAM of 70 ns or faster	L
3	1	80	Ethernet controller, AS delayed one clock	L
4	0	35	Unused by 3VCCPU	P
5	0	35	Unused by 3VCCPU	P
6	N/A	N/A	Used as A19 by 3VCCPU	N/A
7	N/A	N/A	Used as A20 by 3VCCPU	N/A
8	0	35	Unused by 3VCCPU	P
9	0	35	Unused by 3VCCPU	P
10	0	50	Partially used by 3VCCPU	L/P

Table 5- 3VCCPU Wait States

2.5.3.4. TPU Ports

TPU channels 0 through 15, TPUBUS(15:0) are routed from the microprocessor directly to the I/O connector, J4.

2.5.3.5. QSPI Ports

The QSPI chip selects, PCS(3:0), serial data input, QSPI_DIN, serial data output, QSPI_DOUT, and the QSPI clock, QSPI_CLK are routed directly from the microprocessor to the I/O connector, J4

2.5.3.6. Ports E&F

All Port E&F signals are routed from the microprocessor to the I/O connector. Port E bits 7, 6, 5, 4, are defined by the BOOTLOADER and used as bus control signals _SIZ1, _SIZ0, _AS, and _DS respectively in the 3VCCPU design. Port F bits 6:1 are defined as interrupt inputs, IRQ6:1 respectively, IRQ4 is allocated as the interrupt input from IEEE488 interface, IRQ2 is allocated as the interrupt input from Ethernet interface. All other interrupt signals are un-buffered to J4. Port F PF7 and PF0 are used for buzzer signals.

2.5.3.7. FPGA Programming Port

The FPGA programming port consists of a read register and a write register. The write register is 5 bits wide and the read register is three bits wide. Bits 3 and 4 of the write register are OR'ed together in the CPLD and brought out on the CONFIG_OE pin. Refer to Table 3. When LOW, the CONFIG_OE signal tristates off the programming output signals (PDATA, PDCLK, and PNCONFIG) to the FPGA on the Peripheral board. The normal state is to have these signals tristated so that a ByteBlaster can be hooked up on the Peripheral board to program the FPGA manually on the fly. If these signals were not tristated, contention would occur with the ByteBlaster. See register definitions for more details on usage.

2.5.3.8. CPU ID, Peripheral ID, and Software Jumper Interface

The CPU ID, Peripheral ID, and Software Jumper Settings are accessed through a memory mapped register associated with CS10. See register Definitions in Section 2.2.2 for more details.

2.5.4. ETHERNET INTERFACE

The LAN91C96 is a VLSI Ethernet Controller. It contains a Motorola 68000 bus interface and uses an external serial EEPROM to provide a jumperless setup for the Motorola 68000 bus. The LAN91C96 integrates all MAC and physical layer functions, as well as the packet RAM, needed to implement a high performance 10BASE-T (twisted pair) node. Full duplex operation is used to maximize network performance. Isolation transformer U12 is required for the physical link connection to the I/O connector, J2.

The LAN91C96 is used in 100-pin TQFP (1.2 mm body thickness) package. The LAN91C96 operates with a single power supply voltage of 5.0V. See the LAN91C96 register definitions accessing internal registers and packet memory.

2.5.4.1. ETHERNET CONTROLLER INITIALIZATION

The ETHERNET CONTROLLER requires a special initialization procedure. The controller is accessed through CS3 @1WS. Due to the address line wiring, internal registers block starts at offset 300 (hex). CS3 base is set by BOOTLOADER to 300000 by default. Perform the following steps for initialization:

1. Reset ETHERNET CONTROLLER
 - **Write to Ethernet Reset Port (see Section 2.2.2) with a value of 1 on DB0**
 - **wait 100ns**
 - **Write to Ethernet Reset Port (see Section 2.2.2) with a value of 0 on DB0**
2. LONG WORD Write to ETC registers at based Location 0x300300
3. Controller is now initialized

2.5.5. Software Debug Environment

Software can be debugged by connecting a Vision Probe or a VISION ICE to either the on-board BDM port or the BDM port on the Overlay Memory board.

2.5.6. 3VCCPU Pin Descriptions

Signal	I/O	3VCCPU Description
VCC	I	+5V Power input to 3VCCPU
GND	I	+5V return Input to 3VCCPU
NC	N/A	Not Connected
PRFRLDAT(15:0)	I/O	Bi-directional data port
PRFRLAD(20:0)	O	Address output port
TPUBUS(15:0)	I/O	CPU32 Time Processing Unit Channels 0 to 15
TCR2CLK	I	External TPU CLOCK Source or Gate
SYSRESET	O	Active “high” reset Output (Hardware or Software controlled)
_SYSRESETP	O	Active “Low” reset Output (Hardware only controlled)
SFTWRJMPR(7:0)	I	Software Jumpers
PR_W	O	Buffered Read/Write control
PNSTATUS	I	Status Input to FPGA/PLD programming port
PNCONFIG	O	Start Configuration Output from FPGA/PLD programming port
PINIT_DONE	I	Status Input to FPGA/PLD programming port
PDCLK	O	Clock output from FPGA/PLD programming port
PDATA	O	DATA Output from FPGA/PLD programming port
PCONFIG_DONE	I	Status Input to FPGA/PLD programming port
PE7_332	I/O	PORTE from 332 not buffered
PE6_332	I/O	PORTE from 332 not buffered
PE5_332	O	_AS by 3VCCPU overlay, provided to I/O as _AS only, used as the AS input to Ethernet controller also
PE4_332	O	_DS by 3VCCPU overlay, provided to I/O as _DS only, used as DS input to Ethernet controller also
PE3_332	I/O	PORTE from 332 not buffered
PE0_332	I/O	PORTE from 332 not buffered
MODCK	I/O	BEEPER Input Signal
MAN_RST	I	Reset Switch input to 332
ECLK_CS10	O	Unbuffered CS10 from MC68332
BATPLUS	I	Additional battery input to 3VCCPU
_IRQ(7:0)_332	I	Interrupt inputs to 3VCCPU, un-buffered to MC68332
_IDENBIT	O	Enables ID reads for Personality and 3VCCPU ID ports
_DSACK1	I	
_BCS9	O	Buffered CS9 from MC68332
_BCS8	O	Buffered CS8 from MC68332
_BCS5	O	Buffered CS5 from MC68332
_BCS4	O	Buffered CS4 from MC68332
_AVEC	I/O	
TXD	O	Transmit Output from SCI of MC68332 (un-buffered)
RXD	I	Receive Input to SCI of MC68332 (un-buffered)
QSPI_DOUT *	O	QSPI Serial Data Output from MC68332 (un-buffered)
QSPI_DIN *	I	QSPI Serial Data Input to MC68332 (un-buffered)
QSPI_CLK *	O	QSPI Serial Clock
_PCS(3:0) *	O	QSPI Chip selects 0, 1, 2, 3 un-buffered

Table 6- 3VCCPU Pin Description

The QSPI uses seven pins. These pins can be configured for general-purpose I/O when not needed for QSPI application.

2.5.7. J4 Connector I/O Pinout

PRFRLDAT(1)	1	ECLK_CS10	2
PRFRLDAT(2)	3	PRFRLDAT(0)	4
PRFRLDAT(4)	5	_BCS8	6
_PCS0	7	PRFRLDAT(3)	8
VCC	9	VCC	10
PRFRLDAT(7)	11	PRFRLDAT(5)	12
PDCLK	13	PRFRLDAT(6)	14
MODCK	15	PDATA	16
NC	17	NC	18
_SYSRESETP	19	NC	20
NC	21	QSPI_DOUT	22
_IRQ3_332	23	PINIT_DONE	24
NC	25	_PCS3	26
NC	27	_IRQ7_332	28
VCC	29	VCC	30
PNCONFIG	31	RXD	32
PE0_332	33	_PCS2	34
TXD	35	_DSACK1	36
_PCS1	37	_BCS9	38
_IRQ6_332	39	GND	40
_IRQ4_332	41	PRFRLDAT(15)	42
QSPI_CLK	43	PRFRLDAT(14)	44
PRFRLAD(14)	45	PR_W	46
PRFRLDAT(13)	47	PRFRLAD(15)	48
VCC	49	VCC	50
PNCONFIG_DONE	51	PRFRLDAT(12)	52
NC	53	PRFRLAD(12)	54
PRFRLAD(11)	55	PRFRLDAT(11)	56
PNSTATUS	57	PRFRLDAT(8)	58
PRFRLDAT(9)	59	GND	60
QSPI_DIN	61	TCR2CLK	62
PRFRLAD(8)	63	PRFRLDAT(10)	64
_IRQ5_332	65	PRFRLAD(13)	66
PRFRLAD(7)	67	PRFRLAD(10)	68
VCC	69	VCC	70
PRFRLAD(0)	71	PRFRLAD(9)	72
PRFRLAD(5)	73	PRFRLAD(3)	74
PRFRLAD(19)	75	PRFRLAD(6)	76
PRFRLAD(4)	77	PRFRLAD(2)	78
PRFRLAD(18)	79	GND	80
PRFRLAD(17)	81	NC	82
PRFRLAD(1)	83	PRFRLAD(16)	84
TPUBUS(9)	85	TPUBUS(7)	86
TPUBUS(6)	87	NC	88
VCC	89	VCC	90
TPUBUS(10)	91	TPUBUS(12)	92
TPUBUS(8)	93	TPUBUS(13)	94
GND	95	TPUBUS(14)	96

NC	97	_AVEC	98
BATPLUS	99	GND	100
TPUBUS(11)	101	TPUBUS(5)	102
TPUBUS(2)	103	NC	104
NC	105	NC	106
TPUBUS(1)	107	NC	108
VCC	109	VCC	110
TPUBUS(4)	111	NC	112
NC	113	NC	114
NC	115	NC	116
PE5_332	117	PE7_332	118
TPUBUS(3)	119	_BCS8	120
_BCS5	121	PE6_332	122
SYSRESET	123	PE4_332	124
_IRQ1_332	125	_IRQ2_332	126
PRFRLAD(20)	127	MAN_RST	128
VCC	129	VCC	130
PE3_332	131	TPUBUS(15)	132
NC	133	SFTWRJMPR7	134
TPUBUS(0)	135	SFTWRJMPR3	136
NC	137	SFTWRJMPR5	138
SFTWRJMPR4	139	GND	140
SFTWRJMPR0	141	NC	142
SFTWRJMPR1	143	NC	144
SFTWRJMPR6	145	NC	146
SFTWRJMPR2	147	NC	148
VCC	149	VCC	150
_BCS4	151	NC	152
NC	153	NC	154
_IDENBIT	155	NC	156
NC	157	NC	158
GND	159	GND	160
GND	161	NC	162
NC	163	NC	164
NC	165	NC	166
NC	167	NC	168
VCC	169	VCC	170
NC	171	NC	172
NC	173	NC	174
NC	175	NC	176
NC	177	NC	178
GND	179	GND	180

Table 7- J4 Connector Pinout

2.5.8. Example of a Typical 3VCCPU Interface Design

Error! Not a valid link.

Figure 4- Example of a Typical 3VCCPU Design

Note 1:

*Note: Debug Environment :

VisionProbe w/210000148 Overlay plugged into P1 only

OR

Vision ICE Target Head plugged into P1 and P2

OR

VisionProbe plugged into on-board BDM connector

Note 2: CS assignments to peripheral board are flexible and may be assigned as required. Waitstates are assigned according to the unique needs of each peripheral card.

3. 3VCCPU Miscellaneous Design Information

3.1. Interim Test Station Requirements

- **Method for programming the Flash Memory with Boot Loader Code**
 - **Case 1:** Download of Flash with Boot Loader using VisionProbe w/VisionClick Software
 - Test CPU for Supply Shorts , apply power
 - Requires a PC with VisionProbe and VisionClick Software, (overlay memory PCB optional)
 - **Case 2:** Vendor Programming of Flash with Boot Loader
 - Provide a Programmed Part Number for Flash and Boot Loader Software
 - BOM Change to add Programmed Flash Part Number
- **Functional Testing of 3V CPU 2000**
 - Download a 2414 Image (used in this example) using the Down Load Software (across Ethernet or RS232)
 - **Step 1:** Use a 2414 personality Card, with analog board, LCD Display
 - **Step 2:** download 2414 code to CPU 2000 through RS232 and/or Ethernet I/O Ports
 - **Step 3:** boot 3VCCPU
 - This will test all RAM/FLASH Memory onboard
 - CHECK Display (with display bars)
 - Test FPGA download Port by downloading the 2414 FPGA
 - **Step 4:** Use Command Monitor macros on Analog Front end Board , this checks a portion of QSPI Port from 3VCCPU
 - **Step 5:** Run Event input Tests from Command Monitor, this checks a portion of the (TPU Channels)
 - **Step 6:** Run Command Monitor Tests for IEEE488

3.2. TEST SPECIFICATION

1) Required hardware:

- a) PC
- b) 5V Power Source
- c) 2414 Personality Card used for this example.
 - i) Jumper installed in Location 8 of J17 on 2414 to force bootloader execution.
 - ii) Keypad/LCD Display
- d) 3VCCPU PCB
 - i) RS232 Cable or Ethernet Cable

- e) Altera BYTEBLASTER Pod
 - i) BYTEBLASTER Cable Adapter
- f) VisionProbe or VisionICE
 - i) Overlay Memory (optional)
 - ii) BDM Cable Adapter

2) **Required Software:**

- a) VisionClick Software
- b) 2414 Software
- c) Current version of Boot Loader (Version 2.0 RC1)
- d) Loader Application
- e) Altera Programming Software

3) **Procedure to Load CPLD Code:**

- a) Connect BYTEBLASTER w/adapter cable to JTAG connector J5 on 3VCCPU PCB
- b) Startup Altera Programming Software
- c) Select Program File to Download through “File” pull down menu
- d) Apply Power to PCBs
- e) Select the ‘Program’ button
- f) Wait for Altera to verify

4) **Loading BootLoader Version 2.0 (RC1):**

- a) start Hyper terminal (PC application) and set to 38400 baud 8N1.
- b) Apply power to 3VCCPU
- c) In VisionClick Terminal Window enter 'in' at '>ERR>' prompt, wait for the '>BKM>' prompt to appear
 - i) Make sure the correct registers are loaded to emulator flash.
If not, use Tools/ Upload/Download Register files / Download Register Values from File...
 - ii) From the menu, select Tools/Program Flash Devices.
 - iii) Select Host File Name and Path to point to the correct version of Loader.bin
 - iv) Select the correct Flash device (1024 x 16 in 1 device), e.g. AMD 29F160xB
 - v) Make sure Initialize Target Prior to Erase and Erase All or at least Erase to 3FFFF are checked.
 - vi) Set Base Address to 000000 and RAM Workspace Start Address to 200000
 - vii) Select Erase and Program button and wait until programming is finished.
- d) Select the bootloader HyperTerminal
- e) Reboot CPU by cycling Power, a 'chirp' can be heard from the beeper and a message is printed to the HyperTerminal that signifies the correct boot loader version and that ETC Test is “ALL OK”

5) **Example of Procedure to Load 2414 Code:**

- a) Install a 3VCCPU into J15 of 2414 Personality Card with Jumper installed in Location 8 of J17 on 2414 to force bootloader execution.
- b) Install RS232 Cable from PC to J1 of 3V CPU **OR** install the Ethernet cable 441000275 between 3V CPU J2 and a CAT5 **crossover** ethernet cable going to the PC. Alternatively, instrument Ethernet cable can be connected to the same switch/hub as the PC.
- c) If using Ethernet, make sure PC Ethernet card is set to 192.168.0.1. This can be set like this:
 - i) Go to Control Panel → Network Connections and double click on Local Area Connections.

- ii) Dialog box appears. Click on the Properties Button. Another dialog box opens and on the General Tab, Highlight "Internet Protocol (TCP/IP) then click on the Properties button in this dialog box.
- iii) Select the "Use the Following IP Address" and type in 192.168.0.1
- d) Apply power to 3VCCPU and 2414 Personality Card.
- e) start the Loader Application on the PC
 - i) Follow the instructions from the Loader Application. This application will automatically determine that the 3V CPU is plugged into a 2414 personality card and will only allow a 2414 *.sft file to be programmed into the 3V CPU Flash.
 - ii) Select either RS232 download via a COMM port or Ethernet download depending on which cable you have hooked up. If Waters DHCP server is not installed on the PC, manually assign ethernet address 192.168.0.2 to the 3V CPU by doing the following:
 - (1) Connect an RS232 cable to J1 and open a Hyperterminal session.
 - (2) Type the following commands from the prompt in the terminal:


```
CONSOLE> setipflags N F
CONSOLE> setipaddress 192 168 0 2
CONSOLE> netcurrent
CONSOLE> netsaved
```
- iii) start the programming process (either ethernet or RS232)
- iv) wait for Load Complete Message
- v) Remove jumper installed in Location 8 of J17 on 2414
- vi) Reboot CPU by cycling Power
- vii) The 2414 code will run and provide user feedback on LCD Display.

3.3. 3VCCPU Bootloader Register File

TYPICAL EMULATOR REGISTER FILE: (Bootloader Example)

Note: the following section can be cut out of this document into a text document with a *.reg file extension: ex 3VCCPU2000BOOTLOADER.reg

CUT FROM HERE:

CF	TAR	332			
CF	GRP	0003			
SC	MCR	00FFFA00	60CF	SIM	
SC	SYNCR	00FFFA04	0008	SIM	
SC	RSR	00FFFA07	80	SIM	
SC	PORTE	00FFFA11	F3	SIM	
SC	DDRE	00FFFA15	00	SIM	
SC	PEPAR	00FFFA17	F0	SIM	
SC	PORTF	00FFFA19	79	SIM	
SC	DDRF	00FFFA1D	81	SIM	
SC	PFPAR	00FFFA1F	14	SIM	
SC	SYPCR	00FFFA21	0E	SIM	
SC	PICR	00FFFA22	0141	SIM	
SC	PITR	00FFFA24	013C	SIM	
SC	SWSR	00FFFA27	00	SIM	
SC	CSPDR	00FFFA41	08	CHIP SELECTS	
SC	CSPAR0	00FFFA44	2BFF	CHIP SELECTS	
SC	CSPAR1	00FFFA46	03E5	CHIP SELECTS	
SC	CSBARBT	00FFFA48	0007	CHIP SELECTS	

DOCUMENT NO. 810000520 REV. B

SC	CSORBT	00FFFA4A	7830	CHIP SELECTS
SC	CSBAR0	00FFFA4C	1007	CHIP SELECTS
SC	CSOR0	00FFFA4E	7830	CHIP SELECTS
SC	CSBAR1	00FFFA50	2007	CHIP SELECTS
SC	CSOR1	00FFFA52	3C70	CHIP SELECTS
SC	CSBAR2	00FFFA54	2007	CHIP SELECTS
SC	CSOR2	00FFFA56	5C70	CHIP SELECTS
SC	CSBAR3	00FFFA58	3003	CHIP SELECTS
SC	CSOR3	00FFFA5A	7C70	CHIP SELECTS
SC	CSBAR4	00FFFA5C	4003	CHIP SELECTS
SC	CSOR4	00FFFA5E	79B0	CHIP SELECTS
SC	CSBAR5	00FFFA60	5003	CHIP SELECTS
SC	CSOR5	00FFFA62	58B0	CHIP SELECTS
SC	CSBAR6	00FFFA64	FFF8	CHIP SELECTS
SC	CSOR6	00FFFA66	7B81	CHIP SELECTS
SC	CSBAR7	00FFFA68	FFF8	CHIP SELECTS
SC	CSOR7	00FFFA6A	0380	CHIP SELECTS
SC	CSBAR8	00FFFA6C	8003	CHIP SELECTS
SC	CSOR8	00FFFA6E	7970	CHIP SELECTS
SC	CSBAR9	00FFFA70	9003	CHIP SELECTS
SC	CSOR9	00FFFA72	7870	CHIP SELECTS
SC	CSBAR10	00FFFA74	A007	CHIP SELECTS
SC	CSOR10	00FFFA76	7870	CHIP SELECTS
SC	QMCR	00FFFC00	0080	QSM
SC	QTEST	00FFFC02	0000	QSM
SC	QILR	00FFFC04	00	QSM
SC	QIVR	00FFFC05	0F	QSM
SC	SCCR0	00FFFC08	0004	QSM
SC	SCCR1	00FFFC0A	0000	QSM
SC	SCSR	00FFFC0C	0180	QSM
SC	SCDR	00FFFC0E	01FA	QSM
SC	QPDR	00FFFC15	8B	QSM
SC	QPAR	00FFFC16	00	QSM
SC	QDDR	00FFFC17	00	QSM
SC	SPCR0	00FFFC18	0104	QSM
SC	SPCR1	00FFFC1A	0404	QSM
SC	SPCR2	00FFFC1C	0000	QSM
SC	SPCR3	00FFFC1E	00	QSM
SC	SPSR	00FFFC1F	00	QSM
SC	RAMMCR	00FFFB00	0000	RAM
SC	RAMTST	00FFFB02	0000	RAM
SC	RAMBAR	00FFFB04	5000	RAM
SC	TMCR	00FFFE00	0080	TPU
SC	TCR	00FFFE02	0000	TPU
SC	DSCR	00FFFE04	0000	TPU
SC	DSSR	00FFFE06	0000	TPU
SC	TICR	00FFFE08	0000	TPU
SC	CIER	00FFFE0A	0000	TPU
SC	CFSR0	00FFFE0C	0000	TPU
SC	CFSR1	00FFFE0E	0000	TPU
SC	CFSR2	00FFFE10	0000	TPU
SC	CFSR3	00FFFE12	0000	TPU
SC	HSQR0	00FFFE14	0000	TPU
SC	HSQR1	00FFFE16	0000	TPU
SC	HSRR0	00FFFE18	0000	TPU
SC	HSRR1	00FFFE1A	0000	TPU
SC	CPR0	00FFFE1C	0000	TPU
SC	CPR1	00FFFE1E	0000	TPU
SC	CISR	00FFFE20	0000	TPU
SC	LR	00FFFE22	0000	TPU
SC	SGLR	00FFFE24	0000	TPU
SC	DCNR	00FFFE26	0000	TPU

TO ABOVE HERE

NOTE: The CSORBT and CSOR0 register values are setup to use /AS as the strobe for the chip select to solve the hold time violation inherent in legacy 5V CPU2000 boards.

After downloading the *reg file from above , issue a RESET and “cst” command at the background mode prompt in terminal window of the VisionProbe/Ice emulator, and you should see the following :

EXAMPLE:

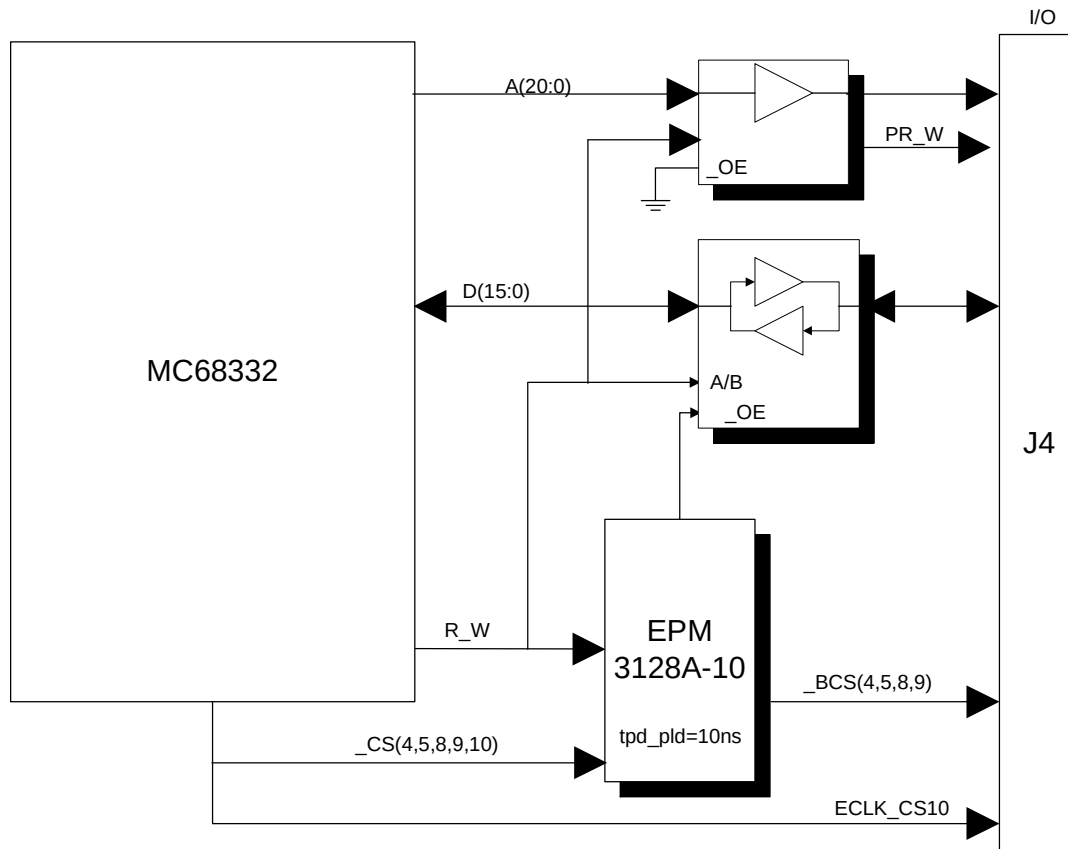
>BKM>cst

Name	Base	Size	Mode	Byte	R/W	Strb	Dsack	Space	IPL	Avec
CSBT	000000	1M	ASync	Both	Both	/AS	0 Wait	S/U	All	OFF
CS0	100000	1M	ASync	Both	Both	/AS	0 Wait	S/U	All	OFF
CS1	200000	1M	ASync	Lower	Both	/DS	1 Wait	S/U	All	OFF
CS2	200000	1M	ASync	Upper	Both	/DS	1 Wait	S/U	All	OFF
CS3	300000	64k	ASync	Both	Both	/DS	1 Wait	S/U	All	OFF
CS4	400000	64k	ASync	Both	Both	/AS	6 Wait	S/U	All	OFF
CS5	500000	64k	ASync	Upper	Both	/AS	2 Wait	S/U	All	OFF
CS6	FFF800	2k	ASync	Both	Both	/AS	F Term	Cpu	All	ON
CS7	FFF800	2k	ASync	Off	Rsvd	/AS	F Term	Cpu	All	OFF
CS8	800000	64k	ASync	Both	Both	/AS	5 Wait	S/U	All	OFF
CS9	900000	64k	ASync	Both	Both	/AS	1 Wait	S/U	All	OFF
CS10	A00000	1M	ASync	Both	Both	/AS	1 Wait	S/U	All	OFF

>BKM>

3.4. Peripheral Connections

Chip Selects 4, 5, 8, 9, 10 are considered peripheral chip selects. The following block diagram shows how to interface to a personality card. Refer to section 2.5.3.3 for Chip Select timing information.



4. APPENDIX

4.1. Flash and SRAM AC Timing

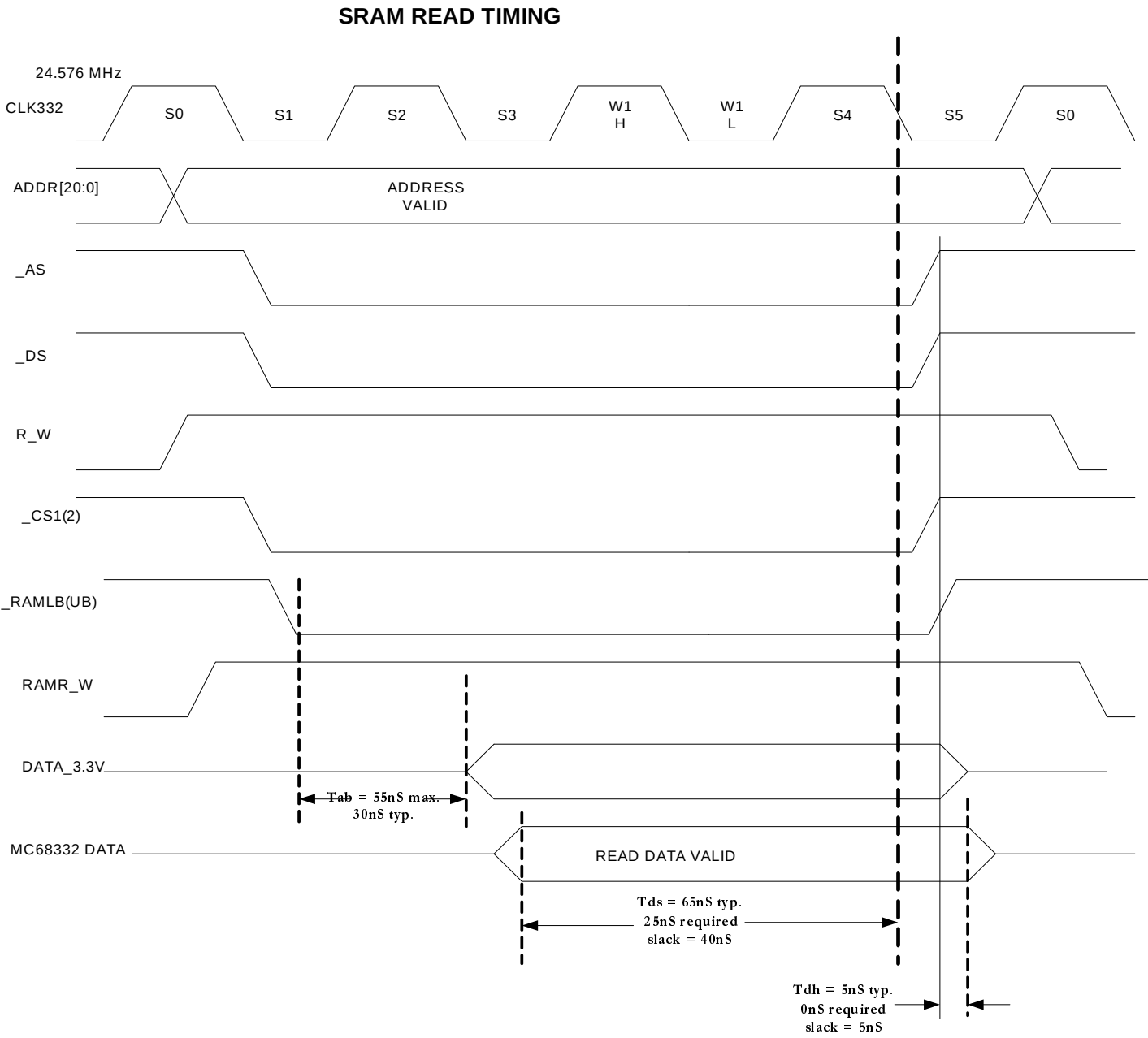


Figure 6- Flash and SRAM AC Timing

SRAM WRITE TIMING

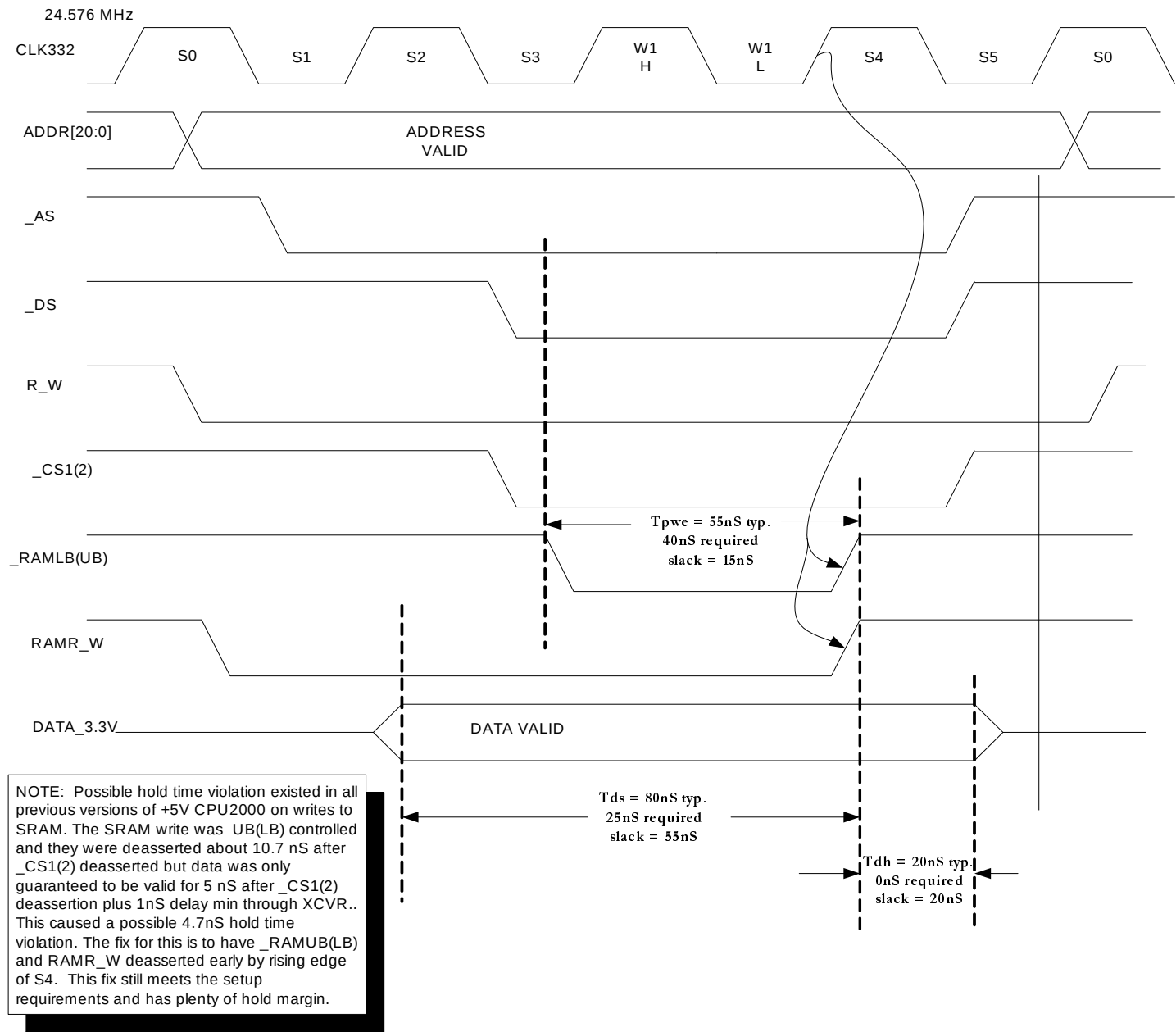


Figure 7 SRAM WriteTiming

FLASH READ TIMING

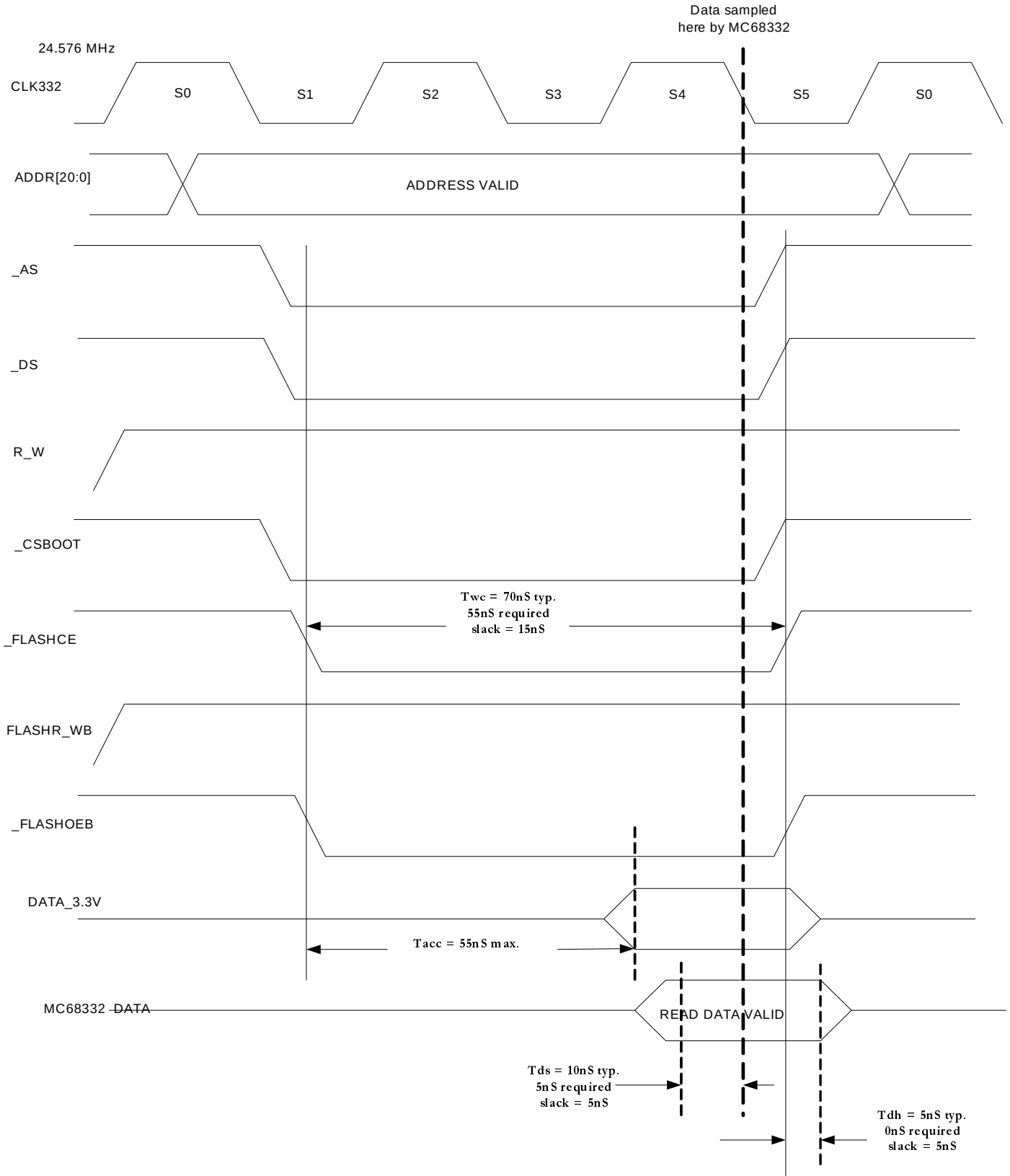


Figure 8- Flash Read Timing

FLASH WRITE TIMING

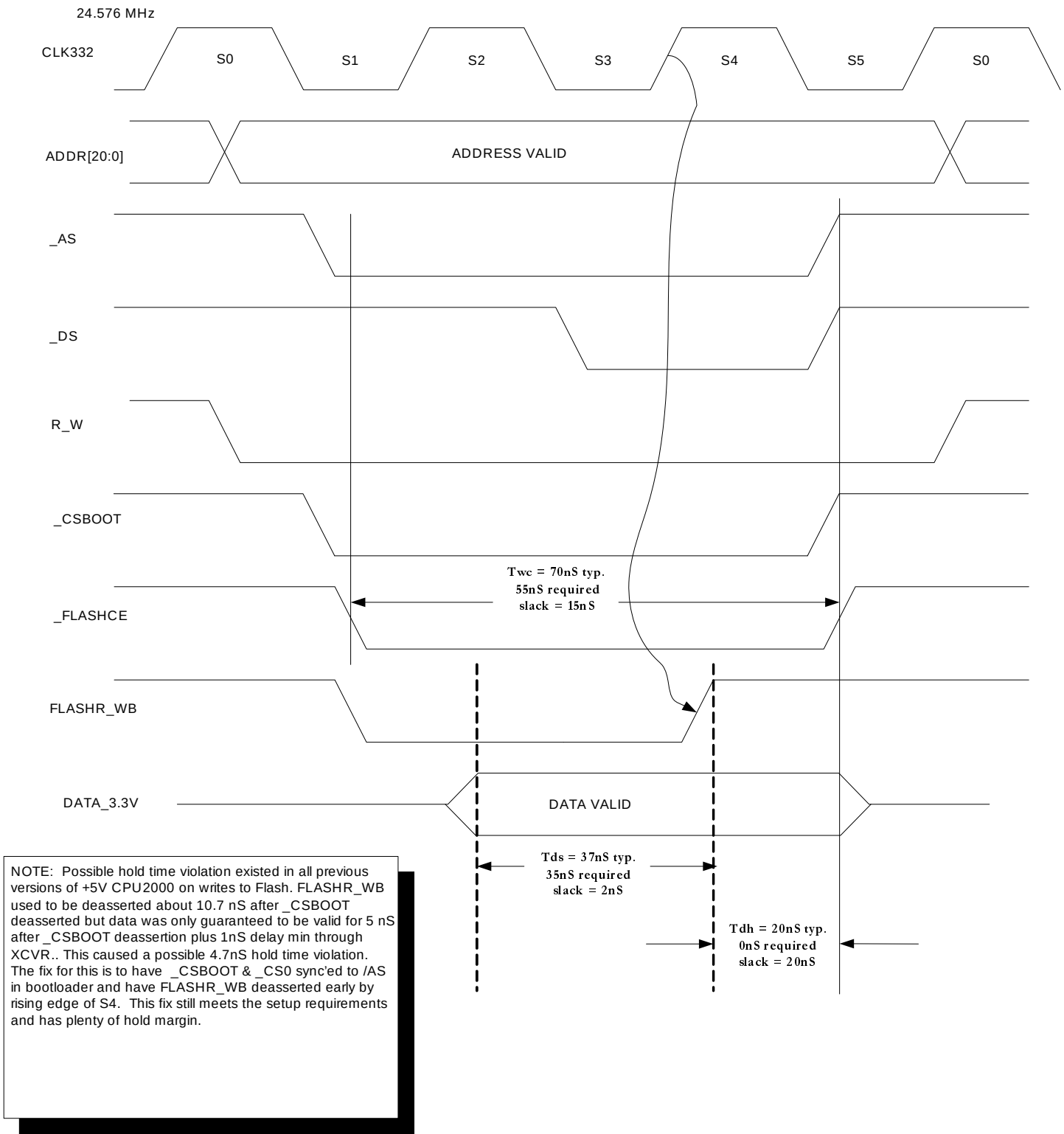


Figure 9- Flash Write Timing