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SUB ASSEMBLY (✓ SIGNATURE REQUIRED)

PRODUCT: PCM / TCM

DOCUMENT NUMBER: 810000456

ASSEMBLY NAME: PCM/TCM Personality
Card

REVISION: A

PART NUMBER AFFECTED: 210000456

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1. INTRODUCTION

1.1 DOCUMENT INTENT

Information in this document will provide a detailed summary of the design criteria ensuring product performance. The intended audiences are Engineers in Software Development, Reliability, Test, Service, Sustaining and Research and Development. The three perspectives considered are performance to the customer, testing of the assembly and future applications of the assembly. Document information will include critical function theory of operation, software control instructions, hardware register definitions, memory map information and I/O electrical specifications. The intent of this document is to provide the reader with additional information not contained in the associated documentation listed in Section 1.3 titled "REFERENCE DOCUMENTATION".

For example, the Assembly Drawing provides connector location while the Schematic provides the connector pin out. The connector location and pin out information will not be redundantly contained in this document. This document does not contain IC specifications unless the IC is being used in an unusual manner.

Note: This is an exact copy of 810000218 with part numbers changed to *10000456 for the RoHS compliant version.

1.2 PRODUCT DESCRIPTION

The goals of the product design were the following:

- To combine the functions of the Pump Control Module and the Temperature Control Module on one printed circuit board.
- To use a common chassis for both instruments.
- Reduce the manufacturing cost of the electronics
- Removal of electronic components that are near obsolescence
- Addition of Ethernet communications.
- Addition of RS232 communications

The following features are also present:

- The IEEE address for the Temperature Control Module can be set via the front panel.
- Field up gradable firmware for the Programmable Logic Device.
- LCD graphics display and membrane key pad on the Temperature Control Module.
- New Chassis design.

The new **PCM/TCM Personality Card** is a single Printed Circuit Board (PCB) that replaces the Temperature Control Module PCB and the Pump Control Module PCB. It is important to note that the PCB is not a multi-function PCB but rather a multi-use PCB. The PCM/TCM Personality Card will not perform the function of both instruments at the same time; different components are populated to perform as either a TCM or a PCM.

1.3 REFERENCE DOCUMENTATION

The following table describes the reference material that applies this document.

Waters Part Number	Description
210000456	Assembly, PCM/TCM Personality Card
710000456	Schematic, PCB, PCM/TCM Personality Card
510000456	PCB, PCM/TCM Personality Card
610000456	Artwork, PCB, PCM/TCM Personality Card
810000142	Performance Specification, CPU2000 Subassembly
711000116	Schematic, FPGA, PCM/TCM Personality Card
810000456	Performance Specification, PCM/TCM Personality Card
*WAT200454	Performance Specification, Pump Controller Module
*WAT038093	Performance Specification, Temp Controller Module

* Applies to original PCM/TCM products - included for reference only.

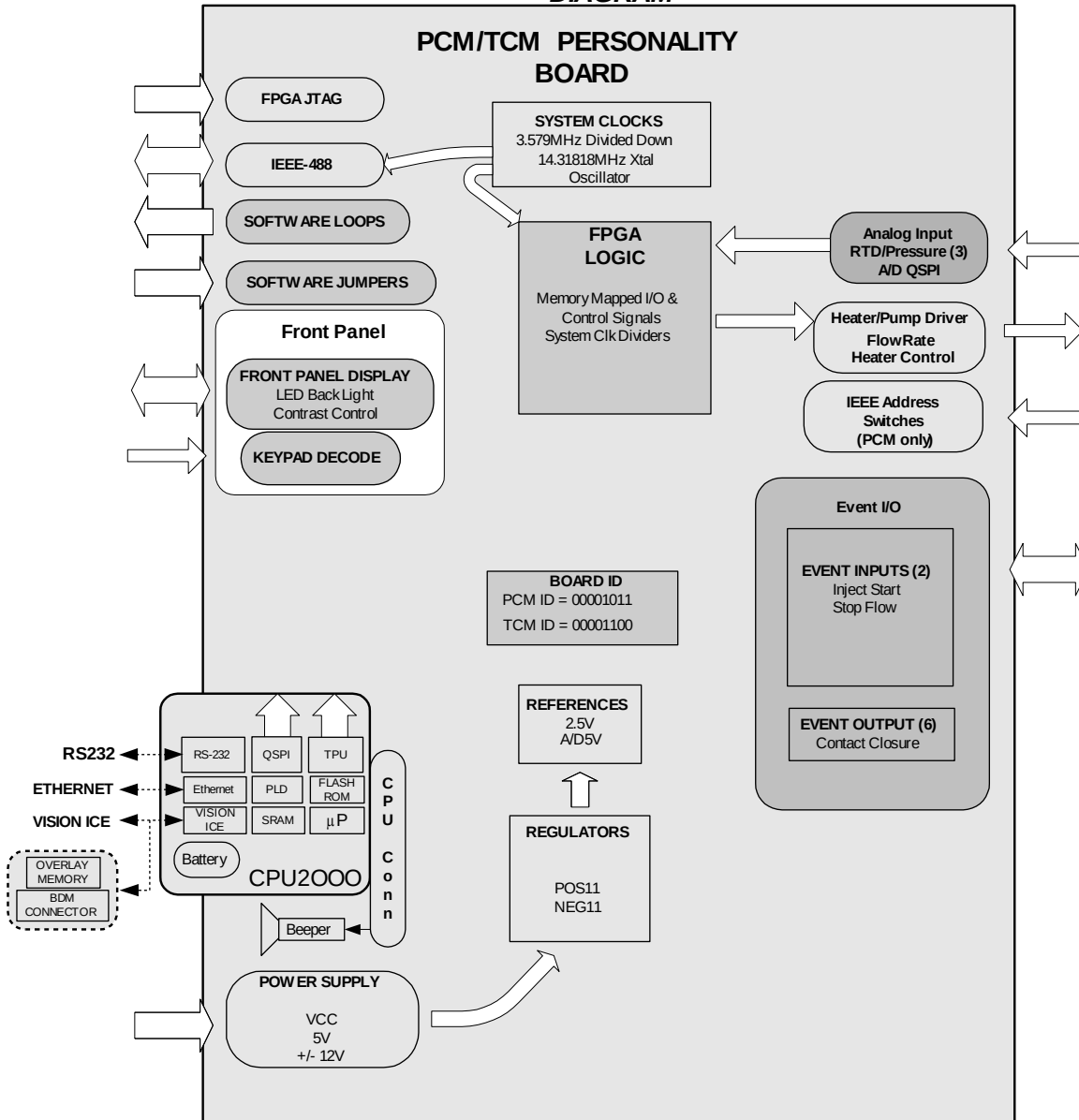
2. HARDWARE DESCRIPTION

This section includes a block diagram for the PCM/TCM (PCB) and Memory map functions of the **TCM/PCM Personality Card**:

FUNCTIONAL BLOCK DIAGRAMS

2.1.1 Block Diagram of PCB

**PCM/TCM PERSONALITY PCB FUNCTIONAL BLOCK
DIAGRAM**



2.2 MEMORY MAP

For the **Overall Memory Map** of the Motorola MC68332, refer to Figure 3-5 of *the Motorola MC68332 User's Manual*. For the **CPU2000 Memory Map**, refer to section 2.1 of the *CPU2000 Performance Specification*.

The following table shows the memory-mapped functions of the **TCM/PCM Personality Card**:

Address	Definition	
400000	Front Panel / Heater	See section 2.3 for the I/O Register Map, and section 2.6 for Circuit Descriptions
500000	I/O Functions	See section 2.3 for the I/O Register Map, and section 2.6 for Circuit Descriptions
800000	IEEE-488	See section 2.6.2 for Circuit Descriptions

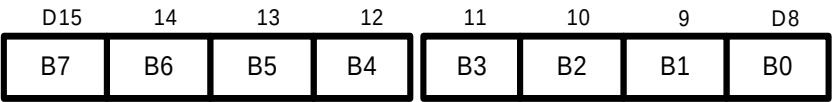
2.3 I/O REGISTER MAP

PCM/TCM I/O Register Map

BCS4

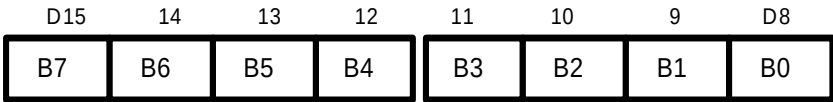
LCD Data Off
(Read/Write)

ADDR[5..0] = [000000]
0x400000



LCD Command Off
(Read/Write)

ADDR[5..0] = [000100]
0x400004



Note: Only “Byte” accesses are permitted.

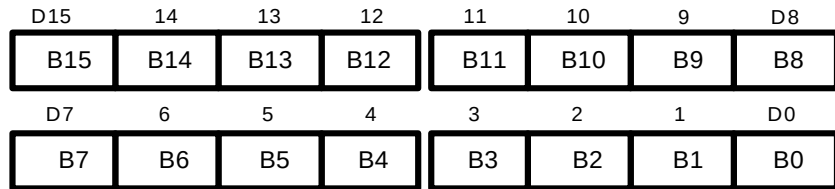
PCM/TCM I/O Register Map

BCS5

PCM = 1*

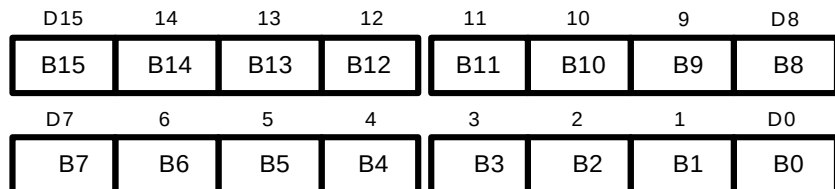
BRM #1 (Read/Write)

ADDR[5..0] = [000000]
0x500000



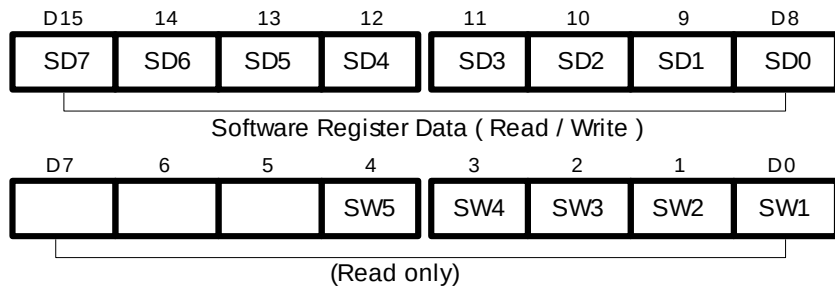
BRM #2 (Read/Write)

ADDR[5..0] = [000010]
0x500002



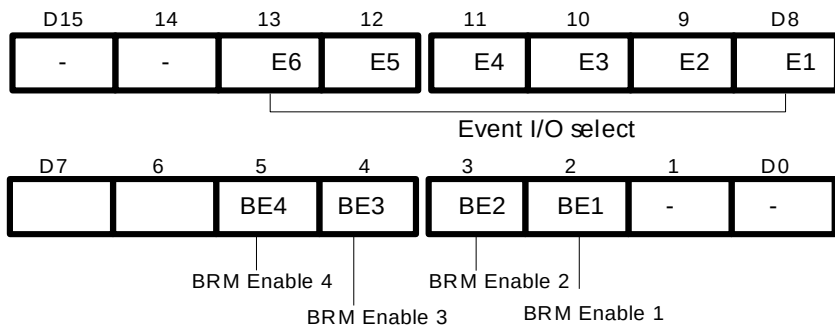
**Software ** /
IEEE-488 Switch ***
Register**

ADDR[5..0] = [000110]
0x500004



**Event IO / Configuration
Register (Read / Write)**

ADDR[5..0] = [000110]
0x500006



* The PCM bit is set high through a pull up resistor on the PCM assembly.
The PCM bit is set low through a pull down resistor on the TCM assembly.

** The Software Register is present for debug purposes, only when connector J3 is mounted on the card.

*** Bits SW1-5 are active “low-level” signals.

For I/O accesses, the “Write” timing requirement is 5 wait states. There are no wait state requirements for a Read.

Note: Only “Word” accesses are permitted.

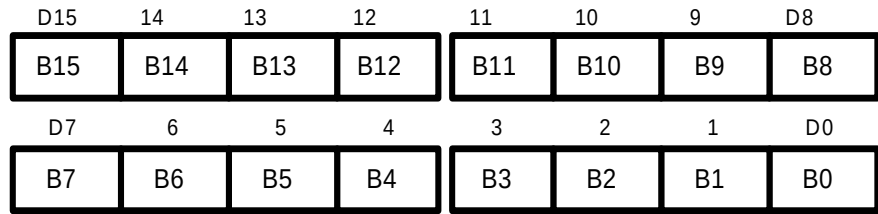
PCM/TCM I/O Register Map

BCS5

PCM = 1*

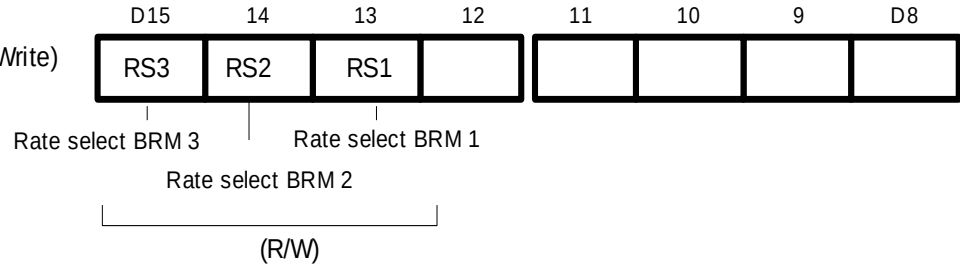
BRM #3 (Read/Write)

ADDR[5..0] = [001000]
(0x500008)



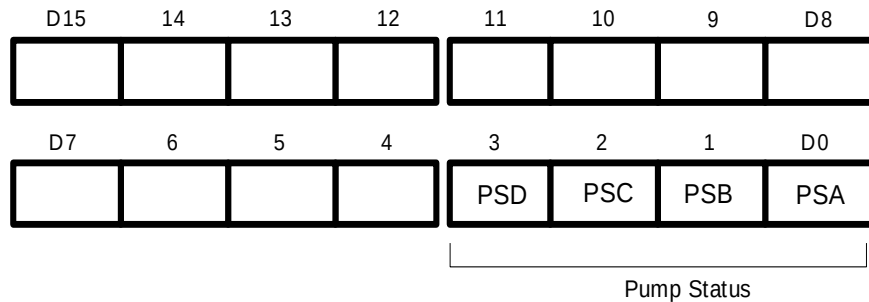
Input Register (Read/Write)

ADDR[5..0] = [001010]
(0x50000A)



Pump Status (Read)

ADDR[5..0] = [001110]
(0x50000E)



* The PCM bit is set high through a pull up resistor on the PCM assembly.
The PCM bit is set low through a pull down resistor on the TCM assembly.

Note: Only “Word” accesses are permitted.

PCM/TCM I/O Register Map

BCS5

PCM = 0*

Keypad Read
(Read)

ADDR[5..0] = [000010]
(0x500002)

D15	14	13	12	11	10	9	D8
			Y5	Y4	Y3	Y2	Y1

Keypad Write
(Write)

ADDR[5..0] = [000010]
(0x500002)

D15	14	13	12	11	10	9	D8
			X5	X4	X3	X2	X1

LCD Contrast
(Write)

ADDR[5..0] = [000011]
(0x500003)

D15	14	13	12	11	10	9	D8
Down	Up						

Column ID1
(Read)

ADDR[5..0] = [011000]
(0x500018)

D15	14	13	12	11	10	9	D8
		ID2B	ID1B	ID0B	ID2A	ID1A	ID0A

Column ID2
(Read)

ADDR[5..0] = [011010]
(0x50001A)

D15	14	13	12	11	10	9	D8
		PCRMC	PCRMB	PCRMA	ID2C	ID1C	ID0C

Heater
(Write)

ADDR[5..0] = [011100]
(0x50001C)

D15	14	13	12	11	10	9	D8
	HTR C	HTR B			HTR A	RTDCAL	

1 = HTR OFF

* The PCM bit is set high through a pull up resistor on the PCM assembly.
The PCM bit is set low through a pull down resistor on the TCM assembly.

Note: Only "Byte" accesses are permitted.

2.3.1 Register Map Description.

LCD Data Off Register Address 0x400000.

B0-B7 8 bit LCD data. Read/write

LCD Command Off Register Address 0x400004.

B0-B7 8 bit LCD data. Read/write

BRM #1 Register. Address 0x500000. Read / Write access

B0-B15 represent the 16 bit digital code that is written to BRM1 to obtain the desired flow rate for pump A.

BRM #2 Register. Address 0x500002. Read / Write access

B0-B15 represent the 16 bit digital code that is written to BRM2 to obtain the desired flow rate for pump B.

BRM #3 Register. Address 0x500008. Read / Write access

B0-B15 represent the 16 bit digital code that is written to BRM3 to obtain the desired flow rate for pump C.

IEEE-488 Register Address 0x500004.

SD0 – SD7 Software register data. This data is Read / Write

SW1-SW5 IEEE Address select bits. These bits are read only.

Event I/O / Configuration Register Address 0x500006.

BE1-BE3 BRM Enable bits for BRM 1, 2 and 3. A high indicates the BRM is enabled. These bits are write with read back capability.

E1-E6 Event I/O select bits. A high indicates that particular Event is selected. These bits are write with read back capability.

Input Register Address 5x0000A

RS1-3 Rate select for BRM1-3. A high selects quarter stepping a low selects full stepping. Write with read back capability.

Pump Status Register Address 0x50000E.

PSA-PSD Pump Status bits for pump A, B and C . A high indicates no pump. During system operation an over pressure condition will cause this bit to go high. These bits are read only.

Keypad Read Register Address 0x500002.

Y1-Y5 Key pad matrix read register bits

Keypad Write Register Address 0x500002.

X1-X5 Key pad matrix write register bits

LCD Contrast Register Address 0x500003.

Up/Run	For the TCM a high on the Up bit will increase the contrast of the display. For the PCM a low on the run bit indicates the instrument run LED is on. Write only
Down/OK	For the TCM a high on the Down bit will decrease the contrast of the display. For the PCM a low on the OK bit indicates the instrument OK LED is on. Write only

Column ID1 Register Address 0x500018.

ID0-2A	Column Heater A Identification Bits. Read only
ID0-2B	Column Heater B Identification Bits. Read only

Column ID2 Register Address 0x500018.

ID0-2C	Column Heater C Identification Bits. Read only
PCRMA-C	Post Column Reaction Module A – C detection bits. A high along with a valid Identification (ID0-2) indicates the column heater present is a PCRM. Read only

Heater Register Address 0x50001C.

HTRA-C	Heater control bits. A high indicates heater off. Write only
RTDCAL	RTD calibration bit. A low switches the current source from RTD0 to a precision resistor to perform calibration measurements.

2.4 QSPI INTERFACE

The QSPI is used sole for acquisitions of data from the Analog to Digital converter. PCS3 is used as the A/D chip select and data is written to the A/D via the MISO (SERIAL_OUT) pin of the QSM and read back from the A/D via the MOSI (SERIAL_IN) pin. The A/D is an ADS8344 16 Bit, 8 Channel SAR . The A/D is used to convert temperature data for the TCM and Pressure data for the PCM. See Section 2.6.3 for more information on the analog to digital conversion.

2.5 TPU CHANNEL DEFINITIONS

TPU Channel	Definition	Direction	Notes
0			
1			
2			
3			
4			
5			
6	Start Injection	Read Only	Sense a “high-going” edge
7	Stop Injection (Stop Flow)	Read Only	Sense a “high-level”
8			
9			
10			
11			
12			
13			
14	A/D Busy	Read Only	Low during conversion (Internal Clock Mode only)

2.6 CIRCUIT DESCRIPTIONS

The **PCM/TCM Personality Card** consists of the functional blocks that are shown in the diagram of section 2.1.1. Each of these blocks is discussed in the following sections.

2.6.1 CPU

The CPU2000 controls the **PCM/TCM Personality Card**, and includes an Ethernet port. Refer to Waters Performance Specification 810000142 for a complete description of the CPU2000. The **TCM/PCM Personality Card** has a JTAG port connector to access the PLD for development purposes. This connector is not populated in production. The ID number of the **PCM Personality Card** assembly is 11 and the ID number of the **TCM Personality Card** assembly is 12.

2.6.2 IEEE-488

The **PCM/TCM Personality Card** supports IEEE-488 communication, using the NAT9914A from National Instruments. The IEEE-488 circuit is identical to that of the original Pump and Temp Controller Modules, except that it operates with a 3.58 MHz clock instead of a 4 MHz clock. The IEEE-488 registers are accessed with **CPU2000** Chip Select 8 and IRQ 4.

2.6.3 Analog In

The **PCM/TCM Personality Card** Uses an ADS8344 16 bit 8 channel SAR analog to digital converter for both pressure and temperature conversion. The ADS8344 has a four wire serial interface compatible with the Motorola 68332 QSPI. Two modes of operation are available for data acquisition, external clock mode and internal clock mode. The PCM/TCM personality card supports both modes.

The ADS8344 has an internal 8 to 1 multiplexer. Prior to the start of each conversion a control byte is written to the device to specify which channel is selected along with a start bit, power down mode select bits and single-ended or differential input select bits. Refer to the manufacturers specification for more detail. The Chart below shows the channel input selection.

Signal Description	Channel	Control Bits		
		A0	A1	A2
Pressure_A / RTD0	Ch 0	0	0	0
Pressure_B / RTD1	Ch 2	0	0	1
Pressure_C / RTD2	Ch 4	0	1	0
RTD CAL	Ch 6	0	1	1
Analog Gnd	Ch 1	1	0	0
Analog Gnd	Ch 3	1	0	1
Analog Gnd	Ch 5	1	1	0
Analog Gnd	Ch 7	1	1	1

Pump Pressure

The Pump pressure input signal range is –10 to 0 VDC which represents a pressure range of 0 to 6000 PSI. The pressure input signal is scaled to 0 to +4.545 VDC using an inverting op-amp with a gain of 0.4545. This represents 757.5uv per psi. The A/D full scale reference voltage for the PCM is 5VDC, this gives a resolution of 76.3uv per bit. The full scale pressure reading of the A/D is.

$$5V(1\text{psi}/757.5\text{uv}) = 6600 \text{ psi}$$

Therefore each LSB represents 0.1 PSI.

Since the A/D specification is 14 bits with no missing codes the effective resolution is 305 μv per bit or 0.403 PSI per bit. The resolution for the existing PCM is 23.4 PSI per bit.

Temperature Channels

There are three temperature compensated constant current sources which develop a voltage across RTDs proportional to temperature for external column heaters. If there are no external heaters installed, the current sources have zeners on their outputs to maintain the current flow so that loading of the internal RTD circuit will not occur. The voltage developed across the RTD's is 0.5 to 0.8VDC and represents a temperature range of 0 to 150 °C. By using a non-inverting op-amp stage with a gain of 5 the RTD voltage is amplified to 2.5 to 4 VDC. The A/D full scale reference voltage for the

TCM is 5VDC. This represents a resolution of 76.3 μ v per bit at 16 bits. Since the temperature range is only 1.5 v of full scale the resolution is 7.63milli degrees C per bit. Since the A/D specification is 14 bits with no missing codes the effective resolution is 0.0305°C per bit. The resolution for the existing TCM is 0.0366 °C per bit.

2.6.4 FPGA Logic

The Logic section contains the circuitry that resides in the EPF6016A Programmable Logic Device (PLD). This device is programmed at power-up by the CPU2000. Refer to section 2.1.2 for the block diagram of this device. The PLD provides the logic for three Bit Rate Multiplier (BRM) circuits, the front panel display and keypad as well as other logic related circuits. Refer to section 2.3 for the I/O Register Map.

BRM Relationship to flow rate

The pumps are controlled by writing to the three Bit Rate Multipliers (BRMs) of the **I/O Register Map** that is shown in Section 2.3 above. The relationship between the digital word that is written to a BRM and the flow rate of a pump is:

Full stepping

$$N = 2000 * \text{Flow (ml/min)} \quad 100 \mu\text{l heads}$$

$$N = 888.89 * \text{Flow (ml/min)} \quad 225 \mu\text{l heads}$$

Where:

N = the digital code that is written to the BRM to obtain the desired flow rate; and
F = the desired flow rate.

The flow rate equation is derived according to the following:

Pump mechanics:	1280 steps/stroke
	100 μ l/stroke
	Full step
Pump displacement:	1280/100 = 12.8 steps/ μ l

BRM clock frequency 3.58 Mhz

2.6.5 Event IO

The Event IO section consists of six SPST relay outputs and two digital inputs.

Digital Inputs

Two event inputs are included in this design. All events are the standard Waters implementation.

Number -	2
Input Voltage -	$\pm$ 30 Volts Maximum
Low Input Voltage	<1.7 Volts
High Input Voltage	>3.2 Volts
Input Filter	RC with τ = 10 msec
Type -	Comparator with State Change Latching
Connector -	Pluggable Terminal Strip
Access -	TPUBUS

Functional Names -	Inject Start	TPUBUS(6)
	Stop Flow	TPUBUS(7)

Event Outputs

The event outputs are normally open relays. Writing a “one” to the signal EVENT_OUT1 performs a Relay closure. During a power-up the relays will be open

Number -	1
Type -	Contact Closure
Voltage -	±30 Volts
Current, Switching -	.5 Amp
Current, Carry -	1.2 Amp
Connector -	Pluggable Terminal Strip

2.6.6 Software Loops

The Software Loops are an initial debug tool that allows the software to write data to a 10-pin header, J7, which also includes VCC and GND. This header is not installed on production cards. Refer to section 2.3 for the I/O Register Map, which is accessed via Chip Select 5 of the **CPU2000**.

2.6.7 Software Jumpers

The Software Jumper logic of the **CPU2000** requires that a header be placed on the personality card. That header is J9 in this design. The Software Jumpers provides a mechanism for accessing debug code during product development. Refer to the **CPU2000 Performance Specification** for more information on the function of the Software Jumpers.

2.6.8 Power

The PCM/TCM personality card is powered by a switching power supply that provides +5VDC and +/- 12VDC.

Power Supply Voltage	Personality Board Current Draw
VCC (+5 VDC)	1.3A
+12 VDC	70mA
-12 VDC	12mA

2.6.9 Heater/Pump Driver

A ULN2003 Darlington Array is used as the driver for the column heaters. This is the same driver used in the 2410 column heaters. The Pump driver circuit uses a 3904 transistor. The population of these drivers are specific to the instrument type. i.e. the pump drivers are populated for the PCM and not for the TCM.

2.6.10 Front Panel

FRONT PANEL LCD DISPLAY DRIVE

Display -	Type -	128 x 64 dot Graphics Display
	Dot Size -	0.48 x 0.48 mm
	Dot Pitch	0.52 x 0.52

	Fluid -	Gray STN
	Viewing Angle -	6 o'clock
	Back Light -	White LED
	Controller -	T6963C
	P/n -	Hitachi HDM64GS12L-W-U1WF
LED Voltage -	8V	
Interface -	Memory Mapped With Direct Access To Pixels By MC68332	
Cable -	20 Pin FFC	

The interface between the display and the MC68332 uses the 6800 synchronous bus cycle. This requires A23 configured for use as ECLK in register CSPAR0 (FFFA44), along with setting the EDIV bit in the register SYNCR (FFFA04) to a 1 (E-clock = system clock divided by 16).

LCD Back Light

The LCD back light is provided from LEDs inside the display. The personality board provides +12v with a current limiting resistors to these LEDs.

Contrast Control

Type -	Uses a DS1669 digital rheostat under software control
Number of Wiper Positions -	64
Minimum Pulse On Time -	1 msec
Maximum Pulse On Time -	1 sec
Repetitive Pulse OFF Time -	1 ms minimum
Write Register -	500003
Register Signals -	UC – up contrast DC – down contrast

Contrast control is provided so that all instrument operators may obtain the optimum LCD contrast over the temperature range of the instrument. LCD contrast varies greatly with viewing angle and temperature.

The negative bias voltage required to control contrast (Vee) is generated by the display. Vee is approximately -9.3 volts when loaded with the contrast control circuit. Unloaded, Vee is approximately -9.8 volts.

At power up, the DS1669 is configured for dual push button operation. The DS1669 is configured for dual push button mode, by having all the control inputs (UC, DC and D) in an open state at power up. In this application, control input D is not used and left open. Control inputs UC and DC are generated from the PLD and is tri-stated during power-up.

The contrast setting is stored in EEPROM in the DS1669. The EEPROM is specified to accept greater than 80,000 writes before wear out. The EEPROM is updated on the first setting change after power up. Subsequent setting changes are stored in the EEPROM only if a change of more than 12.5% is made and the device waits two seconds.

KEYBOARD DECODE

Keypad Matrix Size -	5x4
Interface -	Memory Mapped
Interrupts -	None, Software Polled
Connector/Cable -	10 pin
Write Register -	BCS4001 - Column
Read Register -	BCS4001 - Row
Write Register Signals -	_X1 _X2 _X3 _X4 _X5
Read Register Signals -	_Y1 _Y2 _Y3 _Y4 _Y5

Write the byte sequence 0E, 0D, 0B and 07 to the Keypad Column Register while reading from the Keypad Row Register after every write and checking for a key depress. If no key is depressed, reads a 1F, then continue scanning. If a key is depressed Keypad Row Register then decode the depressed key using the Key Mapping Table. A complete scan through all five columns should be completed fast enough to capture all keys depressed. Reading a value from the Keypad Row Register other than the five codes listed in the Key Mapping Table indicates multiple keys have been depressed and a multiple key error handling algorithm should be used.

Key Mapping -

Step One	Step Two	Step Three
Write Column	Read Row	Decode Pressed Key
0E	1B	UP ARROW
	1D	3
	1E	2
	17	1
	0F	HOME
0D	1B	DOWN ARROW
	1D	6
	1E	5
	17	4
	0F	HELP
0B	1B	ENTER
	1D	CLEAR
	1E	.
	17	0
	0F	MENU
07	1B	Not used
	1D	9
	1E	8
	17	7
	0F	CONFIG

Table 1 Keypad Function Mapping Table

2.6.11 FPGA JTAG

JTAG is used for Programming the PLD on the personality card. The PLD is a SRAM part and needs to be reprogrammed following every power-up. This JTAG port was implemented only for initial debug of this design because on the final design software will program the PLD with a downloaded RBF file. This JTAG connector will be removed from the final BOM but the connector pads will remain on the artwork.

2.6.12 REGULATED POWER SUPPLIES

ANALOG VOLTAGES GENERATED ON BOARD, +11, -11

The Personality PCB requires two analog voltages with their own analog ground isolated from digital ground. The two analog voltages are **+11, -11 VDC** all with a current load requirement of less than 50 mA and a total voltage tolerance of less than $\pm 3\%$. The voltages are generated on the Personality PCB using linear regulators to provide filtering to the analog loads.

2.6.13 VOLTAGE REFERENCES 2.5 V AND 0.106 V

The Personality PCB requires two analog voltage references. Both of these references are tied to Analog Ground (AGND). The analog voltage references are 5V and 2.5 V. The voltage references are generated on the Personality PCB using a LT1236 5V voltage reference and a resistor divider consisting of a 0.1% resistor network. The 2.5V Reference voltage is buffered by an AD712 op-amp in the voltage follower configuration. The 5V Reference voltage is used as the supply voltage and full scale reference voltage for the A/D.

2.6.14 SYSTEM CLOCKS

Crystal Frequency -	14.31818 MHz PLD
Board Divide Down -	3.579 MHz IEEE

The 14.31818 MHz crystal oscillator has is used to drive the PLD. It is also divided down twice to provide a 3.579 MHz clock for IEEE-488.

2.6.15 IEEE Address Switches

The Personality PCB provides a bank of 5 dip switches used to set the IEEE address for the PCM only. These dip switches are not used on the TCM. For the TCM the IEEE address is set via the front panel keypad.

3. ELECTRICAL SPECIFICATIONS

3.1 DATA ACQUISITION

3.1.1 A/D Converter

ADC Input Voltage Range	0 to 5 V, 0-6600PSI,
ADC Transfer Function Pressure	76.3 $\mu\text{V}/\text{LSB}$ (0.1PSI / LSB)
ADC Transfer Function Temperature	76.3 $\mu\text{V}/\text{LSB}$ (0.00763 $^{\circ}\text{C}/\text{LSB}$)
ADC Accuracy	± 2 LSB max. (0.403 PSI) PCM (0.0305 $^{\circ}\text{C}$) TCM
ADC Resolution	16 Bits
Input Filters	1 Pole Low Pass (Analog)
Analog Filter Cutoff Frequency	2832 Hz (PCM) 5Hz (TCM)
Pressure Update Rate	70 KHz max.
Temperature Update Rate	10 hz

3.2 POWER DISSIPATION

Power Connector (J?)	6-Pin Molex
Digital Supply Voltage (VCC)	5 Volts $\pm 5\%$
Digital Supply Current (typ.)	1.3 Amps

Analog Supply Voltage	+/-12 Volts $\pm 5\%$
Analog Supply Current (typ.) (+12V)	70 ma
Analog Supply Current (typ.) (-12V)	12 ma

4. PHYSICAL SPECIFICATIONS

Most of the **PCM/TCM Personality Card** physical dimensions can be found on the PCB Fabrication Drawing.

Weight	261 grams. (without CPU2000)
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5. ENVIRONMENTAL SPECIFICATIONS

Operating Temperature Range	4 to 40 °C
Operating Relative Humidity	10% to 90% (non-condensing)
Storage Temperature Range	-40 to 70 °C
Storage Relative Humidity	0% to 100% (non-condensing)
Forced Air Flow over PCB	None Required

6. SAFETY

The voltages supplied to the **PCM/TCM Personality Card** are +/- 12VDC and +5VDC, which are supplied through the 6-pin J4 connector.