

WATERS CORPORATION

PERFORMANCE SPECIFICATION

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DOCUMENT NUMBER: 810000411

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Document Intent

The intent of this document is to provide performance specifications for the Alliance CPU with Ethernet PCB design. Specifications for software programmers and the system are given. The software model of the Fluidics Driver PCB and the Front Panel PCB are not included in this document. Only the interfaces to these designs are described.

Note: this is an exact copy of 810000319 Rev B with the part numbers changed to *10000411

Related Documents

710000411	Schematic, PCB, Alliance CPU with Ethernet
510000411	PCB, Alliance CPU with Ethernet
610000411	A/W, PCB, Alliance CPU with Ethernet
210000411	Assy, PCB, Alliance CPU with Ethernet

Assembly Description and Intended Use

This is a PCB assembly that is designed to be used in the e2695 product. The Alliance CPU with Ethernet is part of the eProducts initiative which seeks to add Ethernet capability to various instruments in order to supplant IEEE 488 control and data acquisition. The design is implemented using mostly surface mount technology. Most connectors and a few discrete components are through-hole. The design includes a Motorola MC68332 microcontroller and supporting peripherals along with a Analog Devices ADSP2101 DSP. This board interfaces to and controls all of the other circuit boards and peripherals in the instruments. Also, all external instrument interfaces are located on this board. The new Ethernet connectivity is intended to provide a connection to a LAN and data system via an external Ethernet switch. Other Waters Ethernet capable detectors will also be connected to this switch. The Alliance CPU will use Ethernet to load new firmware or boot code into Flash and also to control the instrument. In this regard, the Ethernet will essentially replace the function of the floppy disk and the IEEE 488 interfaces on the Alliance although circuitry will remain on board to support both these interfaces for legacy instruments in the field. There is also an FPGA on board which replaces an obsolete DMA controller and provides Active Check Valve (ACV) control. This Alliance CPU with Ethernet is designed to perform all the functions of its predecessor WAT056370 and in addition, provide signals to drive an Active Check Valve. A new Pump Driver Board with ACV would need to be designed and installed in a e2695 system in order to drive the actual ACV. This Alliance CPU with Ethernet board is backward compatible to existing Alliance systems.

Software Implications

The system SW on the Alliance CPU has major modifications to accommodate new flash density and organization which will accommodate permanently resident boot code. The old WAT056370 Alliance CPU had boot PROMS that were overwritten with the application and it was imperative not to power down the instrument in the middle of that process. The new Alliance CPU will load the boot code into one flash device and the application in the other. No harm is done if power is lost during this process. Other major changes to the software involve adding Ethernet functionality for software and method downloading as well as instrument control. "SYSPREP" capability has also been added. The new Alliance CPU also has the hardware hooks in place for ACV but the code can remain unmodified, since the ACV feature is not implemented in the current e2695 system. The ACV circuitry just resets to the default "off" state. If the ACV feature is ever introduced to the e2695, the following changes are required:

- SW modified to control the ACV
- New Pump Driver with ACV circuitry.
- Active Check Valve itself.

Modified SW will detect that the ACV is present and will initialize the ACV logic.

Block Diagrams

Alliance CPU with Ethernet : Data and Address Bus Structure

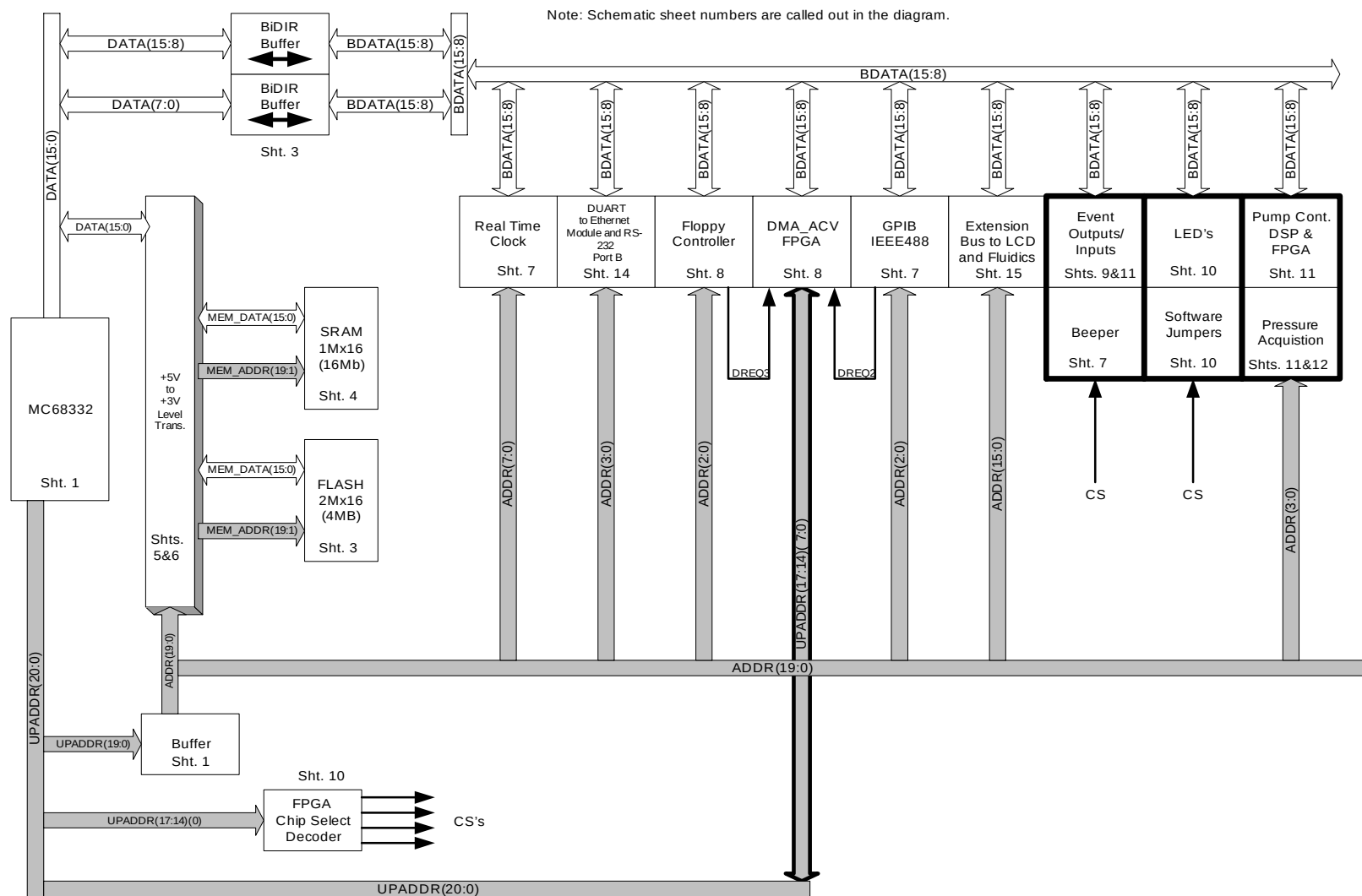


Figure 1
Address and Data Bus Structure

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Figure 2

TPU and Serial Interfaces

Memory Map

Address Range	Device	ACC. SIZE	R/W	DSACK	Size	MC68332 Chip Select
000000 to 0FFFFFF	FLASH	Word	Both	0 Wait	1MB	CSBOOT
100000 to 1FFFFFF	FLASH	Word	Both	0 Wait	1MB	CS3
200000 to 2FFFFFF	SRAM	Word	Both	0 Wait Ext	1MB	CS4
300000 to 3FFFFFF	SRAM	Word	Both	0 Wait Ext	1MB	CS5
400000 to 400007	IEEE488	Byte	Both	6 Wait		CS9
404000 to 40400F	DMAC	Byte	Both	6 Wait		CS9
408000	DMPAGE	Byte	Write	6 Wait		CS9
40C000	EVENT OUT & BEEPER	Byte	Write	6 Wait		CS9
410000	SPARGE & PMPDVR	Byte	Write	6 Wait		CS9
414000	HEX SWITCHES	Byte		6 Wait	16KB	CS9
418000	LEDS	Byte		6 Wait	16KB	CS9
41C000	CLRTCINT	Byte	Both	6 Wait		CS9
420000 to 423FFF	RTC	Byte	Both	6 Wait		CS9
424000 to 427FFF	FDC	Byte	Both	6 Wait		CS9
428000	ACV CURR. THRESHOLD REG.	Byte	Both	6 Wait		CS9
428001	WATCHDOG CURR. THRESHOLD REG.	Byte	Both	6 Wait		CS9
428002	ACV CONTROL REG.	Byte	Both	6 Wait		CS9
428003	ACV STATUS REG.	Byte	Both	6 Wait		CS9
428004	ACV DECAY MODE REG.	Byte	Both	6 Wait		CS9
428005	BOARD REVISION REG.	Byte	Read	6 Wait		CS9
428006	BOARD ID REG.	Byte	Both	6 Wait		CS9
428007	ENET_CNTRL_REG	Byte	Both	6 Wait		CS9
428008 to 42800B	ACV D/A DATA Register	Byte	Write	6 Wait		CS9
428FFF to 42800A	SPARE	Byte	Both	6 Wait		CS9

Address Range	Device	SIZE	R/W	DSACK	Size	Chip Select
429000	SPARE	Byte	Both	6 Wait		CS9
42A000	SPARE	Byte	Both	6 Wait		CS9
42B000	SPARE	Byte	Both	6 Wait		CS9
42C000 to 42C00F	DUART	Byte	Both	6 Wait		CS9
430000 to 433FFF	SPARE	Byte		6 Wait	16KB	CS9
434000 to 437FFF	SPARE	Byte		6 Wait	16KB	CS9
438000 to 43BFFF	SPARE	Byte		6 Wait	16KB	CS9
43C000	EVENT INPUT LATCH	Byte	Read	6 Wait		CS9
43C000	EVENT INPUT BIT CLEAR	Byte	Write	6 Wait		CS9
43C001	EVENT INPUT POLARITY	Byte	Write	6 Wait		CS9
43C002	PRIMARY PRESSURE SET POINT	Word	Write	6 Wait		CS9
43C004	OUTPUT LATCH REGISTER	Byte	Write	6 Wait		CS9
43C002	PRIMARY PRESSURE	Word	Read	6 Wait		CS9
43C004	ACCUMULATOR PRESSURE	Word	Read	6 Wait		CS9
43C006	SAMPLE LOOP PRESSURE	Word	Read	6 Wait		CS9
43C008	DSP CMD/STATUS RX REG	Word	Read	6 Wait		CS9
43C008	DSP CMD/STATUS TX REG	Word	Write	6 Wait		CS9
43C00B	DSP INTERRUPT STATUS	Byte	Read	6 Wait		CS9
43C00B	DSP INTERRUPT MASK	Byte	Write	6 Wait		CS9
43C00C	DSP INTERRUPT CLEAR	Byte	Write	6 Wait		CS9
440001	FLUIDIC MOTORS ENABLE	Byte	Both	8 Wait		CS10
440002	FLUIDIC MOTORS HOLD	Byte	Both	8 Wait		CS10
440005	FLUIDIC CONTROL	Byte	Write	8 Wait		CS10

Address Range	Device	SIZE	R/W	DSACK	Size	Chip Select
440006	FLUIDIC SENSORS 1	Byte	Read	8 Wait		CS10
440007	FLUIDIC SENSORS 2	Byte	Read	8 Wait		CS10
460000 to 467FFF	VIDEO MEMORY	Byte	Both	Ext	32KB	CS7
468000	FRONT PANEL INT STATUS	Byte	Read	Ext		CS7
468001	KEYPAD REGISTER	Byte	Read	Ext		CS7
468001	BACK LIGHT CONTROL	Byte	Write	Ext		CS7
46E000	LCD PAGE REGISTER	Word	Write	Ext		CS7
500000 to 501FFF	68332 RAM	Word	Both	N/A	N/A	N/A
600000 to 6FFFFFF	FLASH	Word	Both	0 Wait	1MB	CS8
FFF000 to FFFFFFF	68332 REGISTERS	Word	Both	N/A	N/A	N/A
FFFFFF (CPU SPACE)	IACK CYCLE	Byte	Read	0 Wait AVEC	2KB	CS0

Microcontroller

This design uses a Motorola MC68332 which is a 32-bit integrated microcontroller. The MC68332 is configured to run at 20 MHz in this design. At the core of the MC68332 is the CPU32 CPU. It is upward code compatible with the MC68010 and includes many of the MC68020 enhancements. The MC68332 also includes intelligent peripheral modules, the time processor unit (TPU), the queued serial module (QSM), and the system integration module (SIM). All of these peripherals are utilized in this design. The MC68332 does all addressing as bytes so when accessing external memories organized as words, the address lines are offset so that A1 of the MC68332 goes to A0 of the memory. The TPU is used to generate stepper motor timing to the drivers on the fluidics driver PCB, generate timing pulses for the gradient proportioning valve (GPV) drivers which are on the pump driver PCB, monitor for the primary pressure event, and to communicate with the bar code reader using asynchronous serial protocol. The QSM consists of two communication interfaces: the queued serial peripheral interface (QSPI) and the serial communications interface (SCI). The QSPI is a synchronous serial interface. It is utilized to interface with all of the options in the system and with the analog output. The SCI is an asynchronous serial interface (UART). It is utilized as a terminal port for software development purposes.

Memory

This design can accommodate up to three megabytes of FLASH and two megabytes of RAM. FLASH is nonvolatile read/write memory. It is utilized to store the system software and data files, such as methods and log files. The FLASH memory is implemented as two 2MB parts which are organized as 1M x 16 bits. Each part contains one 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode). The Bank 1 flash part is selected with _FLASH0CS_LT (CSBOOT) and it is used to store the Boot code and the methods. Since CSBOOT can only access 1MB, this means that only half or 512K x 16 bits of this flash device can be addressed. A signal from the Xilinx FPGA is wired to the upper address bit (A19) of the Bank 1 device as a future provision to access the upper half. No logic currently exists in the Xilinx FPGA to actually drive this address line. The Bank 2 flash part is selected with _FLASH1CS_LT (CS3) or _FLASH2CS_LT (CS8). CS3 accesses the lower 512K x 16 bits and CS8 accesses the upper 512K x 16 bits. Before FLASH memory may be written to, it must be erased. Bank 2 is used to store the firmware application. Erasing may be done on a per sector basis or on an entire part. There is no limit to the number of times a FLASH part may be read. The number of write cycles is limited, however. These parts are expected to last a minimum of 1,000,000 cycles.

The RAM in this design is organized as two 1MB parts. The type of RAM used is called pseudo static RAM. It is different from dynamic RAM in that the address bus does not require multiplexing. Also, the refresh cycle does not require an external address counter. The counter is internal to the part.

Both memory types on this board are designed to operate at zero wait states with the MC68332 running at 20 MHz. To support this, the access speeds for the FLASH and RAM are 70 and 55 nanoseconds respectively. The SRAM memory may be accessed as either bytes or words by the MC68332. The Flash is accessed always as words. These memories are now +3.3V logic and thus require the GTL2000 level translation devices to interface with the rest of the board.

IEEE488

The IEEE488 interface is used for instrument control and data acquisition. It is a standard Waters implementation which uses the 9914 controller. In addition to microprocessor bus cycles, the controller is wired to channel two of the DMA controller for both data reads and writes.

Serial Ports

There are three asynchronous serial ports (UARTs) and one synchronous serial port on the board. Two of the asynchronous ports are implemented in a DUART. The third is part of the MC68332 queued serial module (QSM). The DUART interface is utilized for serial communications to RS232 compatible serial devices via Port A and Port B. Port A RS-232 interfaces with the Digi Connect ME RS-232 to Ethernet Module. This will be explained in more detail in the next section. Port B RS-232 is used for external devices such as printers and the Waters 746 Data Module. There is a cable with a panel mounted DB 9 female connector that plugs in to the CPU card. The DB9 mounts to the CPU card's rear bracket and is used to interface to the external RS-232 devices. The connector is wired to allow for a straight through cable to be used when connecting between this board and a PC. Hardware handshaking is also provided for with the implementation of RTS and CTS. The DUART controller in this design is the SCC2692. The third UART is the serial communications interface (SCI) of the QSM. The QSM consists of two submodules, the SCI is one of them. The SCI is utilized as a terminal port for software development purposes. There is no hardware handshaking implemented with the SCI port, XON/XOFF is used for flow control.

As previously mentioned the QSM consists of two submodules. The SCI and the queued serial peripheral interface (QSPI). The QSPI is a full-duplex synchronous serial interface. It is utilized for communicating with the intelligent options in the system (degasser, heater/cooler, column heater) and with the analog output D/A. In this implementation the MC68332 acts as the master and the peripherals are the slaves. Four select lines are provided by the QSPI for selecting peripherals. They are decoded to address one peripheral at a time. The connectors that the options plug into are all identical. This is possible because the options are able to identify themselves to the MC68332.

Digi Connect ME RS-232 to Ethernet Module (Digi)

This module adds 10/100 Ethernet Capability to the Alliance CPU board. Instrument control and application software and methods will be downloaded via this Ethernet port. IEEE 488 and the floppy disk controller will however still remain on board because the Alliance CPU board must be backward compatible with older legacy systems. Port A RS-232 from the DUART no longer goes out the back panel bracket, but instead is used to communicate to the Digi. The Digi contains an ASIC with an ARM processor that handles the translation from the RS-232 to the Ethernet protocol as well as MAC and PHY circuitry. This module has an RJ-45 jack that is accessed through a cut out in the back panel. The reset to the Digi comes from logic in the Xilinx FPGA and is controlled by firmware. The Digi is held in reset after a power up and firmware must write a "1" to bit (0) of the ENET_CNTRL_REG (0x428007) to release the Digi reset. The reset is released when the e2695 has fully powered up and is in the correct state to accept Ethernet traffic. The firmware can configure the Digi via the RS-232 serial port by asserting Digi DSR which is bit (1) of ENET_CNTRL_REG, prior to releasing the Digi reset. This puts the Digi in a Remote Configuration mode. To exit this configuration mode, the Digi DSR bit is de-asserted and the firmware resets the Digi momentarily. Normal RS-232 communication to the is then enabled.

Floppy Disk Controller (FDC)

This function utilizes a controller that is uPD765A software compatible. The controller is configured to attach to a 3.5 inch 1.44M floppy disk drive. The floppy disk drive should be configured to be selected when drive one is addressed. Due to excessive interrupt latency of the MC68332, the FDC is connected to channel three of the DMA controller for data reads and writes. The FDC is included in this design for backward compatibility reasons only. New e2695 instruments will not have a floppy drive. New application software and methods will be loaded into flash through the Ethernet interface.

Direct Memory Access (DMA)

Direct memory access is provided for the IEEE488 and FDC functions. An 8237A compatible DMA core was written in VHDL and targeted to a Xilinx SPARTAN II +5V tolerant FPGA. In concert with a page address register external to the DMA controller, the DMA controller is designed to access any 64 kilobyte block of the memory in the RAM address space of this board. Channel two is dedicated to the IEEE488 function and channel 3 is dedicated the FDC function. Channels zero and one are not connected to any peripheral, but may be utilized for memory to memory transfers. Due to design constraints the following configuration parameters should be used when configuring the DMA controller:

- DACK sense active low
- DREQ sense active low
- Normal timing
- Single transfer mode
- Address increment

Clocks / Real Time Clock (RTC)

A clock synthesizer is used in this design to generate all the required high frequency clocks. A 25 MHz crystal is the input to this clock synthesizer. The clocks frequencies used in this design from the clock synthesizer are 24 MHz , 20 MHz and 10 MHz as a spare to the new DMA_ACV FPGA.

A 32.768 KHz crystal is an input to the real time clock (RTC) chip. The RTC also outputs a 32.768 KHz clock which is an input to the MC68332 microcontroller after buffering it to the correct CMOS level.. The MC68332 has its own clock synthesizer which is programmed via software to generate a 20 MHz clock. The MC68332 has a 20 MHz clock output which is used for some system functions and is divided down to 10 MHz and 5 MHz for other system functions in a CPLD on board (U26).

The 24 MHz clock from the clock synthesizer is used to drive the floppy disk controller only. The 20 MHz clock from the clock synthesizer is used to drive the DSP in the pump driver control function. The DSP is the only load on this 20 MHz clock due to the clock rise and fall timing parameter constraints of the DSP.

The RTC chip in this design maintains time of day even without power applied. In addition to the time of day function, the RTC chip has 242 bytes of battery backed RAM and a unique 64 bit serial number. The RTC chip is also DS1287 software compatible. The backup battery is a 3.0 volt lithium coin cell located on the circuit board.

Software Jumpers / LED's

Software jumpers are provided for custom configuration control. Eight LED lamps are provided for displaying diagnostic information. The value read from the switches is inverted from the indicted value, and the most significant switch is on top. The LED lamps are turned on by writing a zero to the corresponding bit position, and the most significant LED is on the left

Beeper

An audio transducer is used to generate audible feedback and alarms in this design. The transducer has a built in oscillator that allows for direct voltage operation. The tone generated is at a 2150 Hz frequency. The audio transducer is activated by writing a zero to the corresponding bit position.

Event Inputs / Outputs

Three event inputs and six event outputs are included in this design. The events are the standard Waters implementation. Latches are provided on the event inputs to capture events of short duration. The polarity of the input latches is

programmable. The latches are located in a programmable logic device (PLD). The event outputs are normally open relays. Relay closure is performed by writing a zero to the corresponding bit position.

Analog Output

A dual 16 bit serial digital to analog converter (DAC) and op-amp comprise the analog output circuit. One channel of the dual DAC is for offset adjustment and the other channel is for range. The serial inputs to the dual DAC are connected to the QSPI of the MC68332. The left channel of the DAC is the range and decoded as peripheral chip select 12 of the QSPI. The right channel of the DAC is the offset and decoded as peripheral chip select 13 of the QSPI.

Use the following equations for the analog output:

Va is the analog output voltage
Vo is the offset voltage from the right channel of the DAC, 1.5 to 3.5 volts corresponding to 0 to 65536 DAC counts
Vr is the range voltage from the left channel of the DAC, -1.5 to -3.5 volts corresponding to 0 to 65536 DAC counts
Co is the offset counts loaded into the DAC
Cr is the range counts loaded into the DAC
$$Va = 2 * Vo + Vr$$
$$Co = -32768 + (Vo - 1.5)65536 / 2$$

Pump Driver Control

The pump motors, pump motor encoders, pump seal wash and gradient proportioning valves (GPV) are controlled and monitored via this circuitry. An Analog Devices ADSP2101 DSP clocked at 20 MHz is used to control and monitor the two pump motors and pump motor encoders. A PROM connected to the DSP is used to store the DSP boot program along with SIN and COS tables for driving the motor DACs. The interface between the DSP and each pump motor is a 24 bit parallel to serial register. The outputs of the serial registers are connected to dual 12 bit serial DACs on the pump driver PCB. The pump motor encoders have quadrature outputs. The outputs are decoded by the DSP and motor position is monitored by the DSP. The interface between the DSP and the MC68332 is two 16 bit registers. One register for each direction. The interface to the MC68332 is used to download executable code and for passing commands and status. The pump seal wash is controlled directly by the MC68332. The GPV is controlled by four channels of the TPU in the MC68332.

Active Check Valve Control

All the hooks are in place on the Alliance CPU for Active Check Valve Control. The modifications to the e2695 pump board required for ACV were never implemented however, due to a marketing decision. The following is for informative purposes only.

The Active Check Valve is controlled by the MC68332 , DMA_ACV FPGA (U82) and a D/A converter (U83). Five control signals are derived from this circuitry and are sent over to the Pump Driver Board on a previously unused ACV pin and the 4 sparge lines of the J26 connector. The control signals are:

• ACV_ENB	Output	ACV Enable Bit	1=Enabled; 0= Disabled
• ACV_DIR1	Output	ACV Direction Bit	1= Open; 0=Close
• ACV_LOOP	Input	ACV Presence Indicator.	0=Present; 1=Not Present
• ACV_S_F_DECAY	Output	ACV Slow Fast Decay Bit	0=Fast Decay 1=Slow Decay
• ACV_CURRENT	Output	ACV D/A Output	Used to set ACV Peak current

Firmware first detects whether an ACV is present or not in the Alliance System by reading the ACV_LOOP bit back from the ACV Status Register in the FPGA. If the ACV is present, the firmware will set a Watchdog Current Threshold Register in the FPGA with a peak 8 bit value that the current must never exceed. The firmware then writes an 8 bit value representing one of three distinct operational current levels to the D/A converter. This same 8 bit value is also then written to the ACV Current Threshold Register in the FPGA. The three distinct operational current levels are as follows:

- Plunger/Ball Contact Current Level On the order of ~100 mA. Just enough to have the plunger make contact with the ball.
- Slam Current Level On the order of 1.1 Amps. Plunger slams the ball open.

- Hold Current Level

On the order of 450 mA. Plunger holds ball in the open position.

The FPGA continuously performs a comparison of the ACV Current Threshold Register value and the Watchdog Current Threshold Register value. If the firmware commanded ACV Current should ever exceed the Watchdog current setting, a two second Watchdog timer is started. If the commanded ACV current is dropped down below the watchdog threshold during the 2 second time out, the watchdog timer will be reset. Otherwise the timer will expire and the ACV Enable bit will be cleared and disable the ACV altogether. Firmware can read back the ACV Status Register to see if the watchdog timer has ever expired. An additional level of ACV control is provided by the ACV Slow Fast Decay Bit. In order to achieve the low RMS contact current value from the PWM switching motor controller on the Pump Driver Board, the Fast Decay Mode must be employed. Slow Decay Mode is used for the Slam and Hold Current levels to reduce switching and audible noise.

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Figure 3

Bus Extension Interface

The front panel PCB and the fluidics driver PCB are connected through the bus extension interface. This interface provides two identical 40 pin connectors and buffering for all signals. The data bus width is eight bits and the address range for each of the two chip selects is 64k bytes. This interface also provides buffering for four MC68332 TPU channels which are used by the fluidics driver PCB for driving stepper motors.

Pressure Acquisition / Pressure Event

There are three pressure transducers in the system. One is connected to each of the two pump heads and the third is in the sample loop. The two connected to the pump heads are designated as primary and accumulator. The accumulator transducer always sees system pressure. The primary transducer sees system pressure during transfer and atmosphere during intake periods of the pump cycle. The purpose of the sample loop transducer is to monitor pressure during needle seal pack calibrations. All three transducers are multiplexed into a 16 bit sampling analog to digital converter (ADC). The ADC has a 40 KHz sampling rate and is configured for a 0 to 4 volt input range. The primary transducer is allocated 20 KHz samples and each of the other two transducers is allocated 10 KHz samples each. The transducers are sampled in the order: Primary, Accumulator, Primary, Sample....

The output of the ADC is serial and is connected to custom digital logic that performs simple 8 sample averaging. The averaging logic consists of a 16 bit serial to parallel register, a 19 bit adder, a 19 bit accumulator and three 16 bit result registers. There is one result register for each transducer. After averaging the effective sample rates are 2500 Hz for the primary and 1250 Hz for the accumulator and sample transducers.

The primary transducer is also connected to digital logic that generates a pressure event. The event can be triggered either on rising pressure or falling pressure. The logic consists of a 16 bit set point register and a 16 bit magnitude comparator. The pressure event is setup and controlled by the MC68332. The event goes to the DSP and the TPU. The DSP uses the event for pre-compression before transfer. The TPU uses the event for atmosphere detection on intake.

There are also over pressure detection circuits for the primary and accumulator transducers. Each is set to trip at 3.0 volts or 5500 psi nominal. The trip point is not adjustable. If the transfer function of the transducer changes with time, the pressure that corresponds with 3 volts will change also. If an over pressure is detected it will cause the pump motors to shut down.

DC / DC Converter

The DC/DC converter provides a stable 5 volts for the pressure transducers from 5 volts supplied by the power supply. The conversion is done in two steps. The first is a boost conversion from 5 volts to 7 volts. The second is a linear regulation back down to 5 volts from 7 volts.

Option Interfaces

There are several options that may be added to the base 690/2690 instrument. To date these include: bar code reader, degasser, column heater and heater/cooler. The interface to all the options except the bar code reader is the same. In addition to the bar code reader, up to four other options may be plugged into this board. For these four options, it does not matter which option is plugged into which connector. The options are designed to identify themselves when communicated with. After identification, the software can then configure and control the particular option. A connector that does not have an option plugged into it will identify as a hexadecimal F.

The communication interface to the four options is synchronous serial. The QSPI of the MC68332 is utilized for this interface. Addresses eight through eleven of the QSPI are used for the options. The analog output is the only other function that uses the QSPI and it uses addresses twelve and thirteen. There are several configuration registers in the QSPI. The following bits should be configured as shown to be compatible with the hardware design:

QPDR register	
D6	0
QPAR register	
PCS3	1
PCS2	1
PCS1	1
PCS0	1
MOSI	1
MISO	1
QSM register	
PCS3	1
PCS2	1
PCS1	1
PCS0	1
SCK	1
MOSI	1
MISO	0
SPCR0 register	
MSTR	1
WOMQ	0
CPOL	0
CPHA	0

In addition to the serial interface to the options, a PTC protected 5 volts is also provided for optical isolation purposes.

Two MC68332 TPU channels are used to implement a UART to communicate with the bar code reader. TPU channel 10 is for transmitting and channel 11 is for receiving. No hardware handshaking is provided. This board also provides a PTC protected 5 volts to power the device.

Performance Specifications

Register Definitions

MC68332 Registers

Address: FFFA00 Acronym: SIMCR Name: SIM Configuration Register Initial Value: 63C8			
Bit	Name	Value	Description
15	EXOFF	0	External Clock OFF
14	FRZSW	1	Freeze Software Enable
13	FRZBM	1	Freeze Bus Monitor Enable
12	NOT USED	0	
11	SLVEN	0	Factory Test Mode Enable (Read Only)
10	NOT USED	0	
9	SHEN[1]	1	Show Cycle Enable
8	SHEN[0]	1	
7	SUPV	1	Supervisor/Unrestricted Data Space
6	MM	1	Module Mapping
5	NOT USED	0	
4	NOT USED	0	
3	IARB[3]	1	Interrupt Arbitration Field
2	IARB[2]	0	
1	IARB[1]	0	
0	IARB[0]	0	

Address: FFFA04 Acronym: SYNCR Name: Clock Synthesizer Control Register Initial Value: D300			
Bit	Name	Value	Description
15	W	1	Frequency Control Bit
14	X	1	Frequency Control Bit
13	Y[5]	0	Frequency Control Bits
12	Y[4]	1	
11	Y[3]	0	20.972MHz
10	Y[2]	0	
9	Y[1]	1	
8	Y[0]	1	
7	EDIV	x	E-Clock Divide Rate
6	NOT USED	x	
5	NOT USED	x	
4	SLIMP	x	Limp Mode (Read Only)
3	SLOCK	x	Synthesizer Lock (Read Only)
2	RSTEN	x	Reset Enable For Loss of Crystal
1	STSIM	x	Stop System Integration Module Clock
0	STEXT	x	Stop External Clock

Address: FFFA11 Acronym: PORTE0 Name: Port E Data Register Initial Value: 00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	PE7	0	Not Used
6	PE6	0	Not Used
5	PE5	0	Not Used
4	PE4	0	Not Used
3	PE3	0	DSP Reset 0 = Reset, 1 = Normal Operation
2	PE2	0	Spare I/O
1	PE1	0	Not Used
0	PE0	0	Not Used

Address: FFFA15 Acronym: DDRE Name: Port E Data Direction Register Initial Value: 0C			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	DDE7	0	Bit 07 Direction (1-Out, 0-In)
6	DDE6	0	Bit 06 Direction (1-Out, 0-In)
5	DDE5	0	Bit 05 Direction (1-Out, 0-In)
4	DDE4	0	Bit 04 Direction (1-Out, 0-In)
3	DDE3	1	Bit 03 Direction (1-Out, 0-In) DSP Reset
2	DDE2	1	Bit 02 Direction (1-Out, 0-In) Spare I/O
1	DDE1	0	Bit 01 Direction (1-Out, 0-In)
0	DDE0	0	Bit 00 Direction (1-Out, 0-In)

Address: FFFA17 Acronym: PEPAR Name: Port E Pin Assignment Register Initial Value: F3			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	SIZ1	1	0-I/O,1-SIZ1
6	SIZ0	1	0-I/O,1-SIZ0
5	AS	1	0-I/O,1-AS
4	DS	1	0-I/O,1-DS
3	RMC	0	0-DSP RESET,1-RMC
2	AVEC	0	0-I/O,1-AVEC
1	DSACK1	1	0-I/O,1-DSACK1
0	DSACK0	1	0-I/O,1-DSACK0

Address: FFFA19 Acronym: PORTF0 Name: Port F Data Register Initial Value: 00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	PF7	0	Bit 07 Not Used
6	PF6	0	Bit 06 Not Used
5	PF5	0	Bit 05 Not Used
4	PF4	0	Bit 04 Not Used
3	PF3	0	Bit 03 Not Used
2	PF2	0	Bit 02 Not Used
1	PF1	0	Bit 01 Not Used
0	PF0	0	Bit 00 Not Used

Address: FFFA1D Acronym: DDRF Name: Port F Data Direction Register Initial Value: 00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	DDF7	0	Bit 07 Direction (1-Out, 0-In)
6	DDF6	0	Bit 06 Direction (1-Out, 0-In)
5	DDF5	0	Bit 05 Direction (1-Out, 0-In)
4	DDF4	0	Bit 04 Direction (1-Out, 0-In)
3	DDF3	0	Bit 03 Direction (1-Out, 0-In)
2	DDF2	0	Bit 02 Direction (1-Out, 0-In)
1	DDF1	0	Bit 01 Direction (1-Out, 0-In)
0	DDF0	0	Bit 00 Direction (1-Out, 0-In)

Address: FFFA1F Acronym: PFPAR Name: Port F Pin Assignment Register Initial Value: FF			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	IRQ7	1	0-I/O,1-IRQ7
6	IRQ6	1	0-I/O,1-IRQ6
5	IRQ5	1	0-I/O,1-IRQ5
4	IRQ4	1	0-I/O,1-IRQ4
3	IRQ3	1	0-I/O,1-IRQ3
2	IRQ2	1	0-I/O,1-IRQ2
1	IRQ1	1	0-I/O,1-IRQ1
0	MODCLK	1	0-I/O,1-MODCLK

Address: FFFA21 Acronym: SYPCR Name: System Protection Control Register Initial Value: BC			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	SWE	1	Software Watchdog Enable
6	SWP	0	Software Watchdog Prescale
5	SWT[1]	1	Software Watchdog Timing = 1.0 sec
4	SWT[0]	1	
3	HME	1	Halt Monitor Enable
2	BME	1	Bus Monitor External Enable
1	BMT[1]	0	Bus Monitor Timing = 64 Clocks
0	BMT[0]	0	

Address:		FFFA22	
Acronym:		PICR	
Name:		Periodic Interrupt Control Register	
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED	0	Periodic Request Level
14	NOT USED	0	
13	NOT USED	0	
12	NOT USED	0	
11	NOT USED	0	
10	PIRQL[2]		
9	PIRQL[1]		Periodic Interrupt Vector
8	PIRQL[0]		
7	PIV[7]	0	
6	PIV[6]	1	
5	PIV[5]	0	
4	PIV[4]	0	
3	PIV[3]	0	
2	PIV[2]	0	
1	PIV[1]	0	
0	PIV[0]	0	

Address: FFFA24 Acronym: PITR Name: Periodic Interrupt Timing Register Initial Value: 0029			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED	0	
14	NOT USED	0	
13	NOT USED	0	
12	NOT USED	0	
11	NOT USED	0	
10	NOT USED	0	
9	NOT USED	0	
8	PTP	1	Periodic Timer Prescale 1=Sys Clk/512, 0=Sys Clk/1
7	PITR[7]	0	Periodic Interrupt Timing Modulus
6	PITR[6]	1	
5	PITR[5]	1	=PITR/(System Clock/PTP)/4
4	PITR[4]	0	=41/(32.768KHz/1)/4 = 5.0 msec
3	PITR[3]	0	
2	PITR[2]	0	
1	PITR[1]	1	
0	PITR[0]	0	

Address: FFFA27 Acronym: SWSR Name: Software Service Register Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	SWSR[7]		Bit 07 (Write Only - 55 then AA)
6	SWSR[6]		Bit 06
5	SWSR[5]		Bit 05
4	SWSR[4]		Bit 04
3	SWSR[3]		Bit 03
2	SWSR[2]		Bit 02
1	SWSR[1]		Bit 01
0	SWSR[0]		Bit 00

Address: FFFA41 Acronym: CSPDR Name: Chip Select Pin Data Register Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
6	DO6		Bit 06 Not Used
5	DO5		Bit 05 Not Used
4	DO4		Bit 04 Not Used
3	DO3		Bit 03 Not Used
2	DO2		Bit 02 Not Used
1	DO1		Bit 01 Not Used
0	DO0		Bit 00 Not Used

Address: FFFA44 Acronym: CSPAR0 Name: Chip Select Pin Assignment 0 Register Initial Value: 3F57			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED	0	
14	NOT USED	0	
13	CS5	1	00-I/O,01-FC2,10-CS5(8 bit),11-CS5(16 bit)
12	CS5	1	
11	CS4	1	00-I/O,01-FC1,10-CS4(8 bit),11-CS4(16 bit)
10	CS4	1	
9	CS3	1	00-I/O,01-FC0,10-CS3(8 bit),11-CS3(16 bit)
8	CS3	1	
7	CS2	0	00 or 01-BGACK,10-CS2(8 bit),11-CS2(16 bit)
6	CS2	1	
5	CS1	0	00 or 01-BG,10-CS1(8 bit),11-CS1(16 bit)
4	CS1	1	
3	CS0	0	00 or 01-BR,10-CS0(8 bit),11-CS0(16 bit)
2	CS0	1	
1	CSBOOT	1	10-CSBOOT(8 bit),11-CSBOOT(16 bit)
0	CSBOOT	1	

Address: FFFA46 Acronym: CSPAR1 Name: Chip Select Pin Assignment 1 Register Initial Value: 02B9			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED	0	
14	NOT USED	0	
13	NOT USED	0	
12	NOT USED	0	
11	NOT USED	0	
10	NOT USED	0	
9	CS10	1	00-ECLK,01-A23,10-CS10(8 bit),11-CS10(16 bit)
8	CS10	0	
7	CS9	1	00-I/O,01-A22,10-CS9(8 bit),11-CS9(16 bit)
6	CS9	0	
5	CS8	1	00-I/O,01-A21,10-CS8(8 bit),11-CS8(16 bit)
4	CS8	1	
3	CS7	1	00-I/O,01-A20,10-CS7(8 bit),11-CS7(16 bit)
2	CS7	0	
1	CS6	0	00-I/O,01-A19,10-CS6(8 bit),11-CS6(16 bit)
0	CS6	1	

Address: FFFA48 Acronym: CSBARBT Name: Chip Select Base Address Register Boot ROM Initial Value: 0007			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	0	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA4A Acronym: CSORBT Name: Chip Select Option Register Boot Initial Value: 7870			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	0	
6	DSACK[0]	1	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA4C Acronym: CSBAR0 Name: Chip Select Base Address Register 0 Initial Value: FFF8			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	1	Base Address [23:11]
14	A22	1	
13	A21	1	
12	A20	1	
11	A19	1	
10	A18	1	
9	A17	1	
8	A16	1	
7	A15	1	
6	A14	1	
5	A13	1	
4	A12	1	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	1	
2	BLKSZ[2]	0	
1	BLKSZ[1]	0	
0	BLKSZ[0]	0	

Address: FFFA4E Acronym: CSOR0 Name: Chip Select Option Register 0 Initial Value: 7801			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	0	
6	DSACK[0]	0	
5	SPACE[1]	0	Address Space
4	SPACE[0]	0	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	1	Autovector Enable

Address: FFFA50 Acronym: CSBAR1 Name: Chip Select Base Address Register 1 Initial Value: 4003			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	0	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA52 Acronym: CSOR1 Name: Chip Select Option Register 1 Initial Value: 18B0			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	0	Upper/Lower byte Option
13	BYTE[0]	0	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	1	
6	DSACK[0]	0	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA54 Acronym: CSBAR2 Name: Chip Select Base Address Register 2 Initial Value: 4103			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	1	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1
3	A11	0	
2	BLKSZ[2]	0	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA56 Acronym: CSOR2 Name: Chip Select Option Register 2 Initial Value: 18B0			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	0	Upper/Lower byte Option
13	BYTE[0]	0	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	1	
6	DSACK[0]	0	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA58 Acronym: CSBAR3 Name: Chip Select Base Address Register 3 Initial Value: 1007			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	0	
13	A21	0	
12	A20	1	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA5A Acronym: CSOR3 Name: Chip Select Option Register 3 Initial Value: 7870			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	0	
6	DSACK[0]	1	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA5C Acronym: CSBAR4 Name: Chip Select Base Address Register 4 Initial Value: 2007			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	0	
13	A21	1	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA5E Acronym: CSOR4 Name: Chip Select Option Register 4 Initial Value: 7BF0			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
	MODE	0	Asynchronous/Synchronous Mode
	BYTE[1]	1	Upper/Lower byte Option
	BYTE[0]	1	
	R/W[1]	1	Read/Write
	R/W[0]	1	
	STRB	0	Address Strobe/Data Strobe
	DSACK[3]	1	Data Strobe acknowledge
	DSACK[2]	1	
	DSACK[1]	1	
	DSACK[0]	1	
	SPACE[1]	1	Address Space
	SPACE[0]	1	
	IPL[2]	0	Interrupt Priority Level
	IPL[1]	0	
	IPL[0]	0	
	AVEC	0	Autovector Enable

Address: FFFA60 Acronym: CSBAR5 Name: Chip Select Base Address Register 5 Initial Value: 3007			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	0	
13	A21	1	
12	A20	1	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	
3	A11	0	
2	BLKSZ[2]	1	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA62 Acronym: CSOR5 Name: Chip Select Option Register 5 Initial Value: 7BF0			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	1	Data Strobe acknowledge
8	DSACK[2]	1	
7	DSACK[1]	1	
6	DSACK[0]	1	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA64 Acronym: CSBAR6 Name: Chip Select Base Address Register 6 Initial Value: 4303			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	1	
8	A16	1	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1
3	A11	0	
2	BLKSZ[2]	0	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA66 Acronym: CSOR6 Name: Chip Select Option Register 6 Initial Value: 1830			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	0	Upper/Lower byte Option
13	BYTE[0]	0	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	0	
6	DSACK[0]	0	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA68 Acronym: CSBAR7 Name: Chip Select Base Address Register 7 Initial Value: 4604			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	1	
9	A17	1	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	0	
0	BLKSZ[0]	0	

Address: FFFA6A Acronym: CSOR7 Name: Chip Select Option Register 7 Initial Value: 7BF0			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	1	Data Strobe acknowledge
8	DSACK[2]	1	
7	DSACK[1]	1	
6	DSACK[0]	1	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA6C Acronym: CSBAR8 Name: Chip Select Base Address Register 8 Initial Value: 4807			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	1	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	1	
0	BLKSZ[0]	1	

Address: FFFA6E Acronym: CSOR8 Name: Chip Select Option Register 8 Initial Value: 7870			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	0	
6	DSACK[0]	1	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA70 Acronym: CSBAR9 Name: Chip Select Base Address Register 9 Initial Value: 4005			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	0	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	0	
0	BLKSZ[0]	1	

Address: FFFA72 Acronym: CSOR9 Name: Chip Select Option Register 9 Initial Value: 79B0			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	0	Data Strobe acknowledge
8	DSACK[2]	1	
7	DSACK[1]	1	
6	DSACK[0]	0	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Address: FFFA74 Acronym: CSBAR10 Name: Chip Select Base Address Register 10 Initial Value: 4404			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	A23	0	Base Address [23:11]
14	A22	1	
13	A21	0	
12	A20	0	
11	A19	0	
10	A18	1	
9	A17	0	
8	A16	0	
7	A15	0	
6	A14	0	
5	A13	0	
4	A12	0	Block Size Field 000-2k,001-4k,010-8k,...,111-1M
3	A11	0	
2	BLKSZ[2]	1	
1	BLKSZ[1]	0	
0	BLKSZ[0]	0	

Address: FFFA76 Acronym: CSOR10 Name: Chip Select Option Register 10 Initial Value: 7A30			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	MODE	0	Asynchronous/Synchronous Mode
14	BYTE[1]	1	Upper/Lower byte Option
13	BYTE[0]	1	
12	R/W[1]	1	Read/Write
11	R/W[0]	1	
10	STRB	0	Address Strobe/Data Strobe
9	DSACK[3]	1	Data Strobe acknowledge
8	DSACK[2]	0	
7	DSACK[1]	0	
6	DSACK[0]	0	
5	SPACE[1]	1	Address Space
4	SPACE[0]	1	
3	IPL[2]	0	Interrupt Priority Level
2	IPL[1]	0	
1	IPL[0]	0	
0	AVEC	0	Autovector Enable

Hardware Specific Registers

Address: 408000 (Write Only) Name: DMA Page Register Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	A20		Address for 64K DMA address space
3	A19		
2	A18		
1	A17		
0	A16		

Address: 40C000 (Write Only) Name: Event Output & Beeper Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	Beeper		0=On, 1=Off
6	NOT USED		
5	Event Out 5		Relay Event Output 0=Open, 1=Closed
4	Event Out 4		Relay Event Output 0=Open, 1=Closed
3	Event Out 3		Relay Event Output 0=Open, 1=Closed
2	Event Out 2		Relay Event Output 0=Open, 1=Closed
1	Event Out 1		Relay Event Output 0=Open, 1=Closed
0	Event Out 0		Relay Event Output 0=Open, 1=Closed

Address: 410000 (Write Only) Name: Sparge and PMPDVR Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	Sparge A		Sparge Valve 0=Closed, 1=Open
6	Sparge B		Sparge Valve 0=Closed, 1=Open
5	Sparge C		Sparge Valve 0=Closed, 1=Open
4	Sparge D		Sparge Valve 0=Closed, 1=Open
3	NOT USED		
2	NOT USED		
1	Seal Wash		Seal Wash Solenoid 0=Off, 1=On
0	PDRVRST		Pump Driver Board Reset 0= Operate, 1=Reset

Address: 414000 (Read Only) Name: HEX Switch Input Register Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	SW (7)		Switch Input Port
6	SW (6)		
5	SW (5)		
4	SW (4)		
3	SW (3)		
2	SW (2)		
1	SW (1)		
0	SW (0)		

Address: 418000 (Write Only) Name: LED Output Register Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	LED (7)		LED BIT SET 0=ON, 1=OFF
6	LED (6)		
5	LED (5)		
4	LED (4)		
3	LED (3)		
2	LED (2)		
1	LED (1)		
0	LED (0)		

Address: 428000 (Read/Write) Name: ACV Current Threshold Register Initial Value: 0x00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	ISET (7)		ACV Current Threshold Bits
6	ISET (6)		
5	ISET (5)		
4	ISET (4)		
3	ISET (3)		
2	ISET (2)		
1	ISET (1)		
0	ISET (0)		

Address: 428001 (Read/Write) Name: Watchdog Current Threshold Register Initial Value: 0x00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	WDT (7)		Watchdog Current Threshold Bits – If ACV Current Thres. is set higher than the Watchdog Thres, then 2 second Watchdog Timer starts. When timer expires, ACV is disabled.
6	WDT (6)		
5	WDT (5)		
4	WDT (4)		
3	WDT (3)		
2	WDT (2)		
1	WDT (1)		
0	WDT (0)		

Address: 428002 (Read/Write) Name: ACV Control Register Initial Value: 0x00			
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<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	ACV_DIR1_BIT	1	Direction opens ACV. 0 closes ACV.
0	ACV_ENB_BIT	1	Enables ACV if ISET current is less than WDT current

Address: 428003 (Read Only)			
Name: ACV Status Register			
Initial Value: 0x00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	WDT_Timeout		1 = Watch Dog Timeout. Cleared when ACV_ENB_BIT is set to zero.
0	ACV_LOOP		1 = ACV Not Present 0 = ACV Present

Address: 428004 (Read/Write)			
Name: SLOW or FAST Decay Current Threshold Register			
Initial Value: 0xFF			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	SF_DEC (7)		Slow or Fast Decay Current Threshold Bits – If ACV Current Thres. (ISET) is set higher than the SF_DEC Thres, then we are in SLOW Decay mode. If ACV Current Thres. is set lower than the SF_DEC Thres, then we are in FAST Decay mode.
6	SF_DEC (6)		
5	SF_DEC (5)		
4	SF_DEC (4)		
3	SF_DEC (3)		
2	SF_DEC (2)		
1	SF_DEC (1)		
0	SF_DEC (0)		

Address: 428005 (Read Only)			
Name: Board Revision Register			
Initial Value: 0x41			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	BIT (7)		This register contains the DMA FPGA revision. (i.e. Rev. 1 = 0x01)
6	BIT (6)		
5	BIT (5)		
4	BIT (4)		
3	BIT (3)		
2	BIT (2)		
1	BIT (1)		
0	BIT (0)		

Address: 428006 (Read/Write except bit 6 is Read Only)			
Name: Board ID Register			
Initial Value: 0x00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	BIT (7)		Bit 6 always reads back the opposite of what is written to Bit 7. All other bits read back what was written to them. This register is used by SW to indicate that this is a new Alliance CPU board with Ethernet. Since the old board does not have
6	BIT (6)		
5	BIT (5)		
4	BIT (4)		

3	BIT (3)		this register, invalid data will be read back.
2	BIT (2)		
1	BIT (1)		
0	BIT (0)		

Address: 428007 (Read/Write) Name: Ethernet Control Register Initial Value: 0x00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	DIGI_DSR		Digi DSR Bit . 0=deasserted , 1= asserted. Used to configure Digi Module from serial port.
0	nDIGI_RESET		Digi Ethernet Module Reset. 0=Reset asserted , 1=Reset not asserted.

Address: 428008 to 42800B (Write Only) Name: ACV D/A Register Initial Value: 0x00			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	D2A (7)		D/A Converter data input register. Write the data you want converted to any address in this range.
6	D2A (6)		
5	D2A (5)		
4	D2A (4)		
3	D2A (3)		
2	D2A (2)		
1	D2A (1)		
0	D2A (0)		

Address: 43C000 (Read Only)			
Name: Event Input Latch Register			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	Press Equal		Prim Press Equal 0=Not Equal, 1=Equal
6	Prim Ovr Press		Primary Over Pressure 0=Normal, 1=Error
5	Acc Ovr Press		Accumulator Over Pressure 0=Normal, 1=Error
4	Motors Fail		Pump Motors Over Current 0=Normal, 1=Error
3	NOT USED		
2	Ext Evt In 2		External Event Input 0=No Event, 1=Event
1	Ext Evt In 1		External Event Input 0=No Event, 1=Event
0	Ext Evt In 0		External Event Input 0=No Event, 1=Event

Address: 43C000 (Write Only)			
Name: Event Input Bit Clear			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	Press Equal		Prim Press Equal 0=No Change, 1=Clear
6	Prim Ovr Press		Primary Over Pressure 0=No Change, 1=Clear
5	Acc Ovr Press		Accumulator Over Pressure 0=No Change, 1=Clear
4	Motors Fail		Pump Motors Over Current 0=No Change, 1=Clear
3	NOT USED		
2	Ext Evt In 2		External Event Input 0=No Change, 1=Clear
1	Ext Evt In 1		External Event Input 0=No Change, 1=Clear
0	Ext Evt In 0		External Event Input 0=No Change, 1=Clear

Address: 43C001 (Write Only)			
Name: Event Input Polarity Register			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	Press Equal		Prim Press Equal 0 for rising, 1 for falling
6	Prim Ovr Press		Primary Over Pressure Set to 1
5	Acc Ovr Press		Accumulator Over Pressure Set to 1
4	Motors Fail		Pump Motors Fail Set to 0
3	NOT USED		
2	Ext Evt In 2		External Event Input 0=0 Active, 1=1 Active
1	Ext Evt In 1		External Event Input 0=0 Active, 1=1 Active
0	Ext Evt In 0		External Event Input 0=0 Active, 1=1 Active

Address: 43C002 (Write Only)			
Name: Pressure Event Set Point Register			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	PPSP15		MSB Pressure Event Set Point
14	PPSP14		
13	PPSP13		
12	PPSP12		
11	PPSP11		
10	PPSP10		
9	PPSP9		
8	PPSP8		
7	PPSP7		
6	PPSP6		
5	PPSP5		
4	PPSP4		
3	PPSP3		
2	PPSP2		
1	PPSP1		
0	PPSP0		LSB Pressure Event Set Point

Address: 43C004 (Write Only)			
Name: Output Latch Register			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	PSCLKEN		Primary Shift Clock Enable 0=Disable, 1=Enable
6	Press Evt En		Pressure Event Enable 0=Disable, 1=Enable
5	MOTORS ON		Pump Motors On 0=Motors Off, 1=Motors On
4	SMPLXDCRGND		Sample Loop Xdcr Ground 0=Normal/Open, 1=Ground
3	NOT USEDV		
2	NOT USED		
1	NOT USED		
0	NOT USED		

Address: 43C002 (Read Only)			
Name: Primary Pressure			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	PP15		Primary Pressure MSB
14	PP14		
13	PP13		
12	PP12		
11	PP11		
10	PP10		
9	PP9		
8	PP8		
7	PP7		
6	PP6		
5	PP5		
4	PP4		
3	PP3		
2	PP2		
1	PP1		
0	PP0		Primary Pressure LSB

Address: 43C004 (Read Only)			
Name: Accumulator Pressure			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	AP15		Accumulator Pressure MSB
14	AP14		
13	AP13		
12	AP12		
11	AP11		
10	AP10		
9	AP9		
8	AP8		
7	AP7		
6	AP6		
5	AP5		
4	AP4		
3	AP3		
2	AP2		
1	AP1		
0	AP0		Accumulator Pressure LSB

Address: 43C006 (Read Only)			
Name: Sample Loop Pressure			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	SLP15		Sample Loop Pressure MSB
14	SLP14		
13	SLP13		
12	SLP12		
11	SLP11		
10	SLP10		
9	SLP9		
8	SLP8		
7	SLP7		
6	SLP6		
5	SLP5		
4	SLP4		
3	SLP3		
2	SLP2		
1	SLP1		
0	SLP0		Sample Loop Pressure LSB

Address: 43C008			
Name: DSP Command/Status Register			
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	DSP15		DSP Command/Status Register MSB
14	DSP14		
13	DSP13		
12	DSP12		
11	DSP11		
10	DSP10		
9	DSP9		
8	DSP8		
7	DSP7		
6	DSP6		
5	DSP5		
4	DSP4		
3	DSP3		
2	DSP2		
1	DSP1		
0	DSP0		DSP Command/Status Register LSB

Address: 43C00B (Read Only)			
Name: DSP Interrupt Status Register			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	RXERRORINT		DSP Rx Command/Status Register Overrun Interrupt
2	RXFULLINT		DSP Rx Command/Status Register Full Interrupt
1	TXEMPTYINT		DSP Tx Command/Status Register Empty Interrupt
0	DSPINT		DSP Chip Interrupt

Address: 43C00B (Write Only)			
Name: DSP Interrupt Mask Register			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	RXERRORMSK		Rx Overrun Int Mask 0=Enable, 1=Disable
2	RXFULLMSK		Rx Full Int Mask
1	TXEMPTYMSK		Tx Register Empty Int Mask 0=Enable, 1=Disable
0	DSPIMSK		Chip Interrupt Mask 0=Enable, 1=Disable

Address: 43C00C (Write Only)			
Name: DSP Interrupt Clear Register			
Initial Value: XX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	RXERRORCLR		DSP Receive Reg Overrun Int Clear 0=NC, 1=CLEAR
2	RXFULLCLR		DSP Receive Reg Full Int Clear 0=NC, 1=CLEAR
1	TXEMPTYCLR		DSP Transmit Reg Empty Int Clear 0=NC, 1=CLEAR
0	NOT USED		

Interrupt Priorities

<u>Level</u>	<u>Assignment</u>
6	DUART
5	Keypad/Door Switch
4	DSP
3	DMA TC
2	GPIB
1	Floppy Disk Drive

Microprocessor

Manufacturer	Motorola
Chip Part Number	MC68332
Chip Frequency	20 MHz

Memory

FLASH

Size	(2) 16 megabit chips
Organization	(3) 1 megabyte segments
Access Size	Word
Access Speed	70 nsec, 0 wait states @ 20 MHz

Battery Backed

Size	242 bytes
Access Type	I/O port
Access Size	Byte
Access Speed	450 nanoseconds / transfer

Pseudo Static RAM

Size	(2) 8 megabit chips
Organization	(2) 1 megabyte segments
Access Size	Word or Byte
Access Speed	55 nsec (read), 0 wait states @ 20 MHz

Flash and SRAM Static Timing

name	min	max	margin	comment
tchav	0	23	na (delay)	delay from clock high to address valid
tahct573	7.5	7.5	na (delay)	address delay through AHCT573 buffers
tglt	5.5	5.5	na (delay)	delay through GTL200 Level Translators
tclas	0	23	na (delay)	delay from clock low to AS low
tclds	0	23	na (delay)	delay from clock low to DS low
tchrw	0	23	na (delay)	delay from clock high to R_W Asserted
tchainv	0	23	na (delay)	delay from clock high to address invalid
tclasneg	2	23	na (delay)	AS,CS and DS negated
tpdu26	8.3	8.3	na (delay)	Altera 7032 comb. delay. (tio+tpia+tlad+tpexp+tcomb+tc
tfloedat	35	35	na (delay)	delay from Flash OE to read data from Flash
tficsdz		16	na (delay)	delay from Flash CS de-asserted to Data HiZ
tsroedat	25	25	na (delay)	delay from SRAM OE to read data from SRAM
tsrcsdz	20	20	na (delay)	delay from SRAM CS de-asserted to Data HiZ
SAMPLE0	0	0	na (sample)	Point where MC68332 samples SRAM Read Data
tSU	5		0.187	Setup time margin for SRAM Read Data
SAMPLE1	0	0	na (sample)	Point where MC68332 samples Flash Read Data
tfISU	5		13.074	Setup time margin for Flash Read Data
tregu26	6.5	6.5	na (delay)	Altera 7032 register to output delay. (tin+tglob+th+tcomb
tdvds	10		na (delay)	data valid to data strobe
tclds	0	23	na (delay)	delay from clock low to CS low
tfwrSU	45		23.266	Setup time margin for Write data to Flash
tsrwrSU	25		43.266	Setup time margin for Write Data to SRAM

IEEE488

Manufacturer	National Instruments
Chip Part Number	NAT9914
Chip Frequency	5MHz
Number	1
Controller	NAT9914
Drivers	75ALS160/75ALS161

Serial Ports

Type	RS232
Number	3
Connectors	(1) 9 Pin D-Sub, Receptacle
Controllers	(2) SCC2692 DUART
	(1) MC68332 SPI
Flow Control	(2) RTS,CTS
	(1) XON/XOFF
Drivers	MAX233

FLOPPY DISK CONTROLLER

Number	1
Manufacturer	National Semiconductor
Chip Part Number	DP8473
Chip Frequency	24 MHz
Connector	34 Pin IDC Header
Interface Type	Standard Floppy Disk Drive
Controller	National Semiconductor DP8473

DMA

Manufacturer	Waters Custom FPGA
Chip Part Number	Xilinx XC2S50
Chip Frequency	20 MHz
Channel Assignments	Channel 1: Not Used Channel 2: Not Used Channel 3: IEEE488 Channel 4: Floppy Disk Controller
Address Range	Any 64k Block within The SRAM Space

Clocks / Real Time Clock

Real Time Clock

Manufacturer	Dallas Semiconductor
Chip Part Number	DS1685
Software Model	Compatible with DS1287
Chip Frequency	32 KHz

Clock Generator

Manufacturer	IDT
Chip Part Number	ICS343MPLF
Chip Input Frequency	25 MHz
Derived Frequencies	20MHz, 24 MHz

Switches / LED's

Beeper

Manufacturer	Star
Part Number	SCC2692
Audible Frequency	3.6864 MHz
Sound Level	85 dB @ 10cm
Resonant Frequency	2299 Hz

Event Inputs / Outputs

Event Inputs

Number	3
Type	Comparator
Connector	Pluggable Terminal Strip
Input Voltage Range	± 30 volts
Input High Voltage	>3.0 volts ±10%
Input Low Voltage	<1.9 volts ±10%
Minimum Pulse Width	10 milliseconds

Event Outputs

Number	6
Type	Relay , SPST N.O.
Connector	Pluggable Terminal Strip
Type	Contact Closure
Maximum Voltage	200 volts DC
Maximum Current	0.5 amps DC
Contact Resistance	0.2 ohms

Analog Output

Number	1
Connector	Pluggable Terminal Strip
Type	Voltage
Voltage Range	2 volts
Minimum Voltage	0.06 volts @ 1mA
	0.53 volts @ 15 mA
Maximum Voltage	4.1 volts @ 1 mA
	3.84 volts @ 15 mA

Pump Driver Control

DSP Memory Map

<u>Space</u>	<u>Address</u>	<u>Read/Write</u>	<u>Function</u>
Data	0x0000	R	Primary Motor Encoder State
Data	0x0001	R	Accumulator Motor Encoder State
Data	0x0002	R	Interrupt Events
Data	0x0002	W	Clear Interrupt Events
Data	0x0003	R	Host Interface DSP Input Register (16 bits)
Data	0x0003	W	Host Interface DSP Output Register (16 bits)
Data	0x0004	W	Accumulator Motor COS Register (12 bits, 11 thru 0)
Data	0x0005	W	Accumulator Motor SIN Register (12 bits, 11 thru 0)
Data	0x0006	W	Primary Motor COS Register (12 bits, 11 thru 0)
Data	0x0007	W	Primary Motor SIN Register (12 bits, 11 thru 0)
Data	0x0008	W	Control Register
Data	0x0400 to 0x37FF	R	EPROM Square Root Table (16 bits)
Data	0x3800 to 0x39FF	R/W	On-chip Data Memory (16 bits)
Data	0x3C00 to 0x3FFF	R/W	On-chip Control Registers (16 bits)
Boot	0x0000 to 0x03FF	R	EPROM DSP Boot Program (8 bits, 15 thru 8)
Program	0x0000 to 0x03FF	R/W	On-chip Program Memory (24 bits)

DSP Hardware Registers

Address: DM 0x0000 Read Only			
Name: Primary Motor Encoder State			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	NOT USED		
10	NOT USED		
9	NOT USED		
8	NOT USED		
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	PHASE A		Primary Motor Encoder Phase A
0	PHASE B		Primary Motor Encoder Phase B

Address: DM 0x0001 Read Only			
Name: Accumulator Motor Encoder State			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	NOT USED		
10	NOT USED		
9	NOT USED		
8	NOT USED		
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	PHASE A		Accumulator Motor Encoder Phase A
0	PHASE B		Accumulator Motor Encoder Phase B

Address: DM 0x0002 Read Only			
Name: Interrupt Event Register			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	NOT USED		
10	NOT USED		
9	NOT USED		
8	NOT USED		
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	TX REG EMPTY		Transmit Register Empty, 1 Active
3	RX REF FULL		Receive Register Empty, 1 Active
2	PRESSEVENT		Primary Pressure Event, 1 Active
1	PENCHE		Primary Encoder Changed, 1 Active
0	AENCHE		Accumulator Encoder Changed, 1 Active

Address: DM 0x0002 Write Only			
Name: Clear Interrupt Events			
Initial Value: XXXX			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	NOT USED		
10	NOT USED		
9	NOT USED		
8	NOT USED		
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	TX REG EMPTY		Transmit Register Empty, 1=Clear, 0=No Change
3	RX REF FULL		Receive Register Empty, 1=Clear, 0=No Change
2	PRESSEVENT		Primary Pressure Event, 1=Clear, 0=No Change
1	PENCHE		Primary Encoder Changed 1=Clear, 0=No Change
0	AENCHE		Accumulator Encoder Changed 1=Clear, 0=No Change

Address: DM 0x0004 Write Only			
Name: Accumulator Cos			
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	Cos11		Accumulator Motor Cos
10	Cos10		
9	Cos9		
8	Cos8		
7	Cos7		
6	Cos6		
5	Cos5		
4	Cos4		
3	Cos3		
2	Cos2		
1	Cos1		
0	Cos0		

Address: DM 0x0005 Write Only			
Name: Accumulator Sin			
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	Sin11		Accumulator Motor Sin
10	Sin10		
9	Sin9		
8	Sin8		
7	Sin7		
6	Sin6		
5	Sin5		
4	Sin4		
3	Sin3		
2	Sin2		
1	Sin1		
0	Sin0		

Address: DM 0x0006 Write Only			
Name: Primary Cos			
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	Cos11		Primary Motor Cos
10	Cos10		
9	Cos9		
8	Cos8		
7	Cos7		
6	Cos6		
5	Cos5		
4	Cos4		
3	Cos3		
2	Cos2		
1	Cos1		
0	Cos0		

Address: DM 0x0007 Write Only			
Name: Primary Sin			
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	Sin11		Primary Motor Sin
10	Sin10		
9	Sin9		
8	Sin8		
7	Sin7		
6	Sin6		
5	Sin5		
4	Sin4		
3	Sin3		
2	Sin2		
1	Sin1		
0	Sin0		

Address: DM 0x0008 Write Only			
Name:			
Initial Value:			
<u>Bit</u>	<u>Name</u>	<u>Value</u>	<u>Description</u>
15	NOT USED		
14	NOT USED		
13	NOT USED		
12	NOT USED		
11	NOT USED		
10	NOT USED		
9	NOT USED		
8	NOT USED		
7	NOT USED		
6	NOT USED		
5	NOT USED		
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	PRESSEVTDSBL		Pressure Event Disable 1= Disable, 0= Enable
0	DSPINT		DSP Interrupt Set 1= Set, 0= Clear

DSP

Manufacturer	Analog Devices
Chip Part Number	ADSP2101
Chip Frequency	20 MHz

Position Encoders

Number	2
Connector	10 Pin IDC Header
Supply Voltage	5 Volts $\pm 5\%$
Supply Current (each)	100 mA
Receiver	26LS32
Encoder Output	Differential Quadrature
Encoder Resolution	500 Counts Per Revolution
Clockwise Rotation (viewed From Rear)	Phase B leads Phase A

Pump Driver PCB Interface

Number	1
Connector	24 Pin D-Sub
Interface Type	Custom Serial and Parallel
Interface Drivers	74ABT573
Functions Controlled	Active Check Valve Gradient Proportioning Valves (4) Seal Wash Solenoid Pump Pump Motors (2) Pump Driver PCB Reset
Functions Monitored	Motors/Fan Fail ACV Presence Indicator

Gradient Proportioning Valves

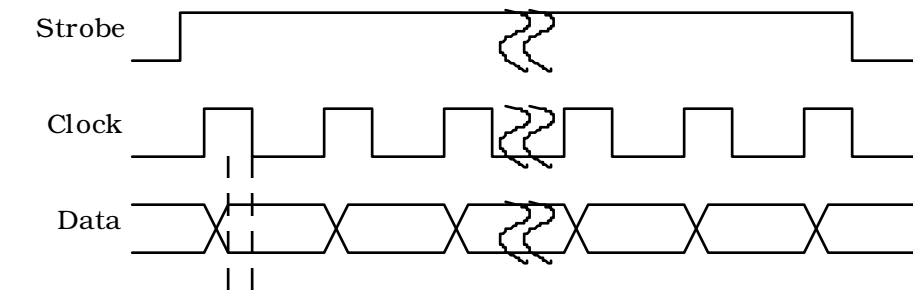
Number	4
Signal Polarity	Active High
Minimum Pulse Width	5 milliseconds
Maximum Pulse Width	None
Minimum Cycle Time	10 milliseconds

Seal Wash Solenoid Pump

Signal Polarity	Active High
Minimum Pulse Width	50 milliseconds
Maximum Pulse Width	1 second
Minimum Cycle Time	500 milliseconds

Pump Motors

Signal Polarity	Active High
Data Format	Sin 23-12 Cos 11-0, MSB First
Transfer Function	0xFFFF = 4.13 Amps 0x100 = 0.0 Amps 0x000 = -4.13 Amps
LSB Weighting	.002018 Amps
Clock Frequency	2 MHz Gated
Clock Duty Cycle	60%
Data Valid to Clock Low	170 nanoseconds minimum

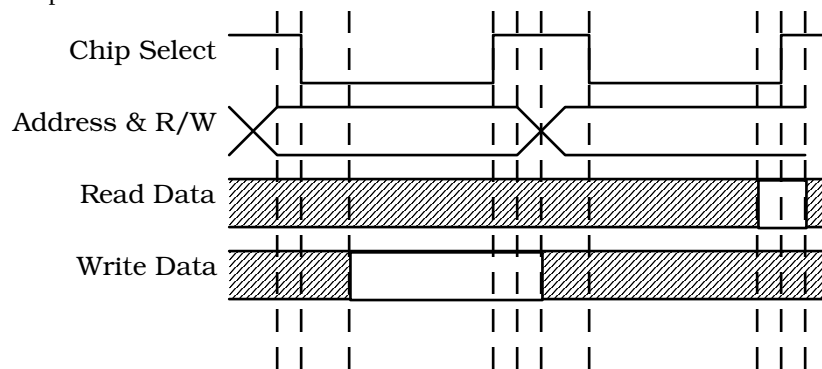


Pump Driver PCB Reset

Signal Polarity	Active High
Minimum Pulse Width	10 microseconds
Reset Duration	3 seconds

Bus Extension Interface

Number	2
Connector	40 Pin IDC Header
Interface Type	Extension of Microprocessor
Interface Drivers	74ABT573
Data Bus Width	8 Bits
Address Space Range	64K Bytes
Interrupt	Single, Shared, Low Active, Level
Address Valid to Chip Select Asserted	0 nsec minimum
Chip Select Negated to Address Invalid	8 nsec minimum
Chip Select Asserted to Valid Data (Write)	58 nsec maximum
Chip Select Negated to Data Invalid (Write)	8 nsec minimum
Data Valid to Chip Select Inactive (Read)	15 nsec minimum
Chip Select Negated to Data Invalid (Read)	0 nsec minimum
Chip Select Pulse Width	720 nsec minimum



Pressure Acquisition / Pressure Event

Pressure Transducers Interface

Number	3
Connector	4 Pin Shielded Data Link
Supply Voltage	5 Volts
Supply Current (each)	<25 mA
Input Impedance	>2 megaohm
ADC Input Voltage Range	0 to 4 volts
ADC Digital Resolution	16 Bits
ADC Transfer Function	16384 lsb/volt
Input Filters	2 Pole Low Pass (Analog) 8 Sample Average (Digital)
Analog Filter Cutoff Frequency	225 Hz
Sample Loop Pressure Update Rate	1250 Hz
Primary Pressure Update Rate	2500 Hz
Accumulator Pressure Update Rate	1250 Hz
Transducer Output Voltage Range	0.5 to 3.0 volts
Transducer Pressure Range	0 to 5500 psi
Transducer Transfer Function	2200 psi/volt

Option Interfaces

Bar Code Reader Interface

Number	1
Connector	15 Pin Double Density D-Sub, Receptacle
Interface Type	RS232 (Tx and Rx Only) with Supply Voltage
Data Rate	Programmable
Supply Voltage	5 V $\pm 5\%$
Maximum Supply Current	.5 A, Protected with .75 A PTC

Other

Number	4
Type	Synchronous Serial With Supply Voltage
Connector	8 pin
Supply Voltage	5 $\pm 5\%$ volts
Maximum Supply Current	0.5 amps, protected with 0.75 amps PTC

DC / DC Converter

Input Voltage	5 $\pm 5\%$ volts
Output Voltage	4.94 $\pm 2.5\%$ volts
Input Regulation	.04%
Output Current	50 mA

Power Input

Connector	4 Pin Molex
Logic Supply Voltage	5 Volts $\pm 5\%$
Logic Supply Current	1.5 amps (without options)
Analog Supply Voltage	5 Volts $\pm 5\%$
Analog Supply Current (max.)	0.2 amps (with pressure transducers)

Physical

Length	12 in
Width	8 in
Height	1.5 in
Weight	20.5 oz without rear plate and hardware

Environmental

Operating	
Temperature Range	0 to 40 °C
Humidity Range	10 to 90% (non-condensing)
Storage	
Temperature Range	-40 to 70 °C
Humidity Range	0 to 100% (non-condensing)