

A

B

C

D

E

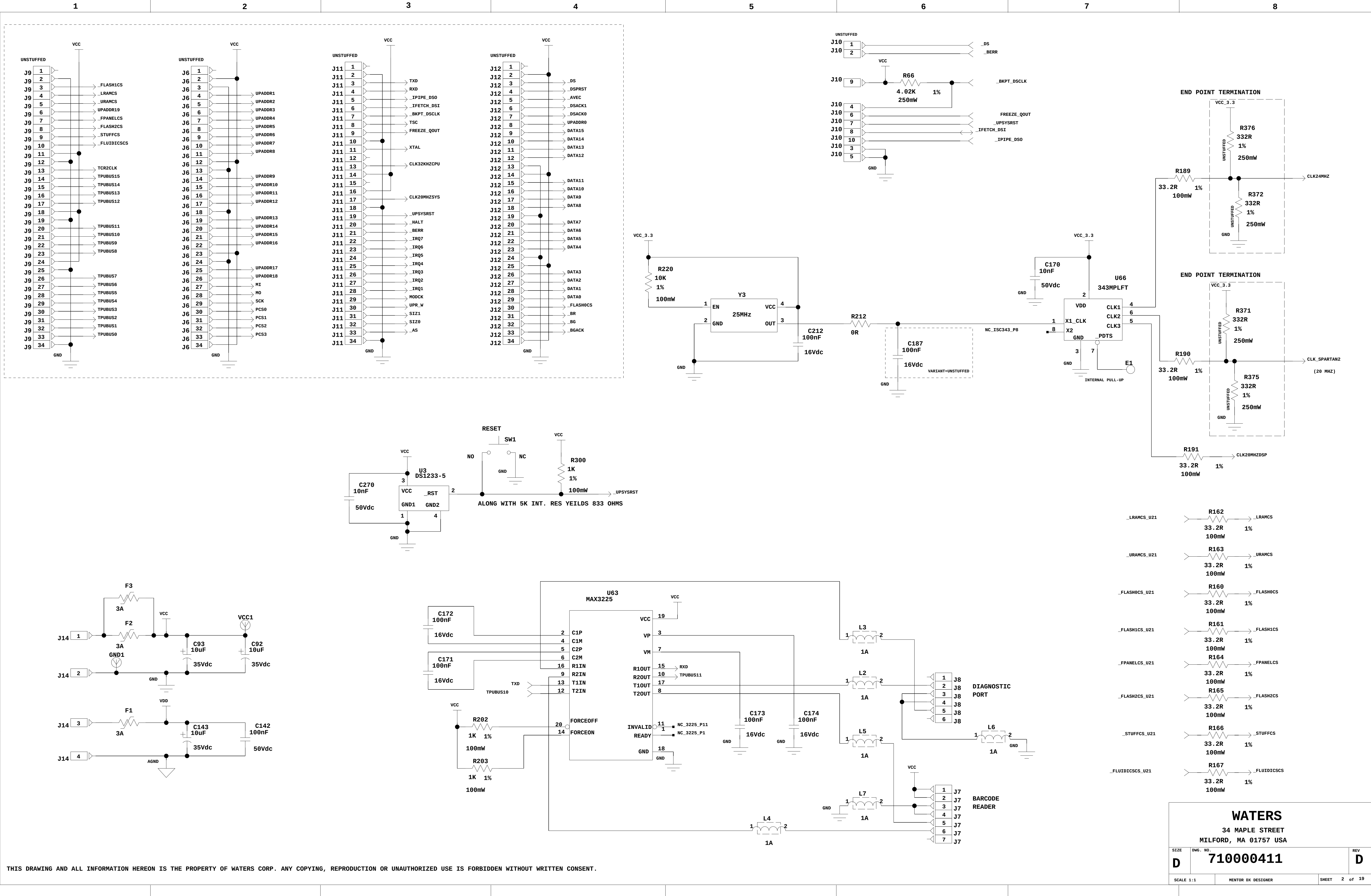
A

B

C

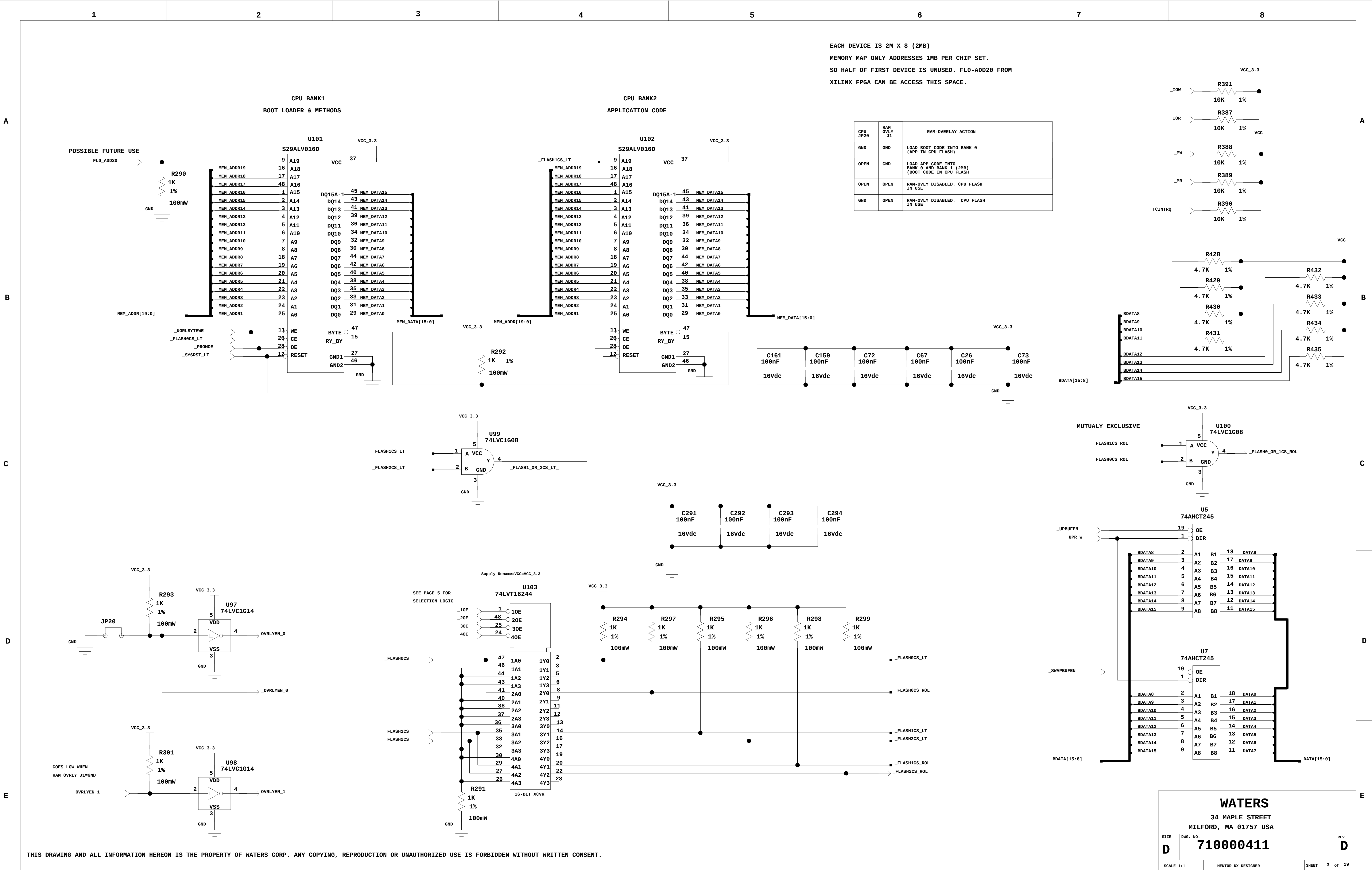
D

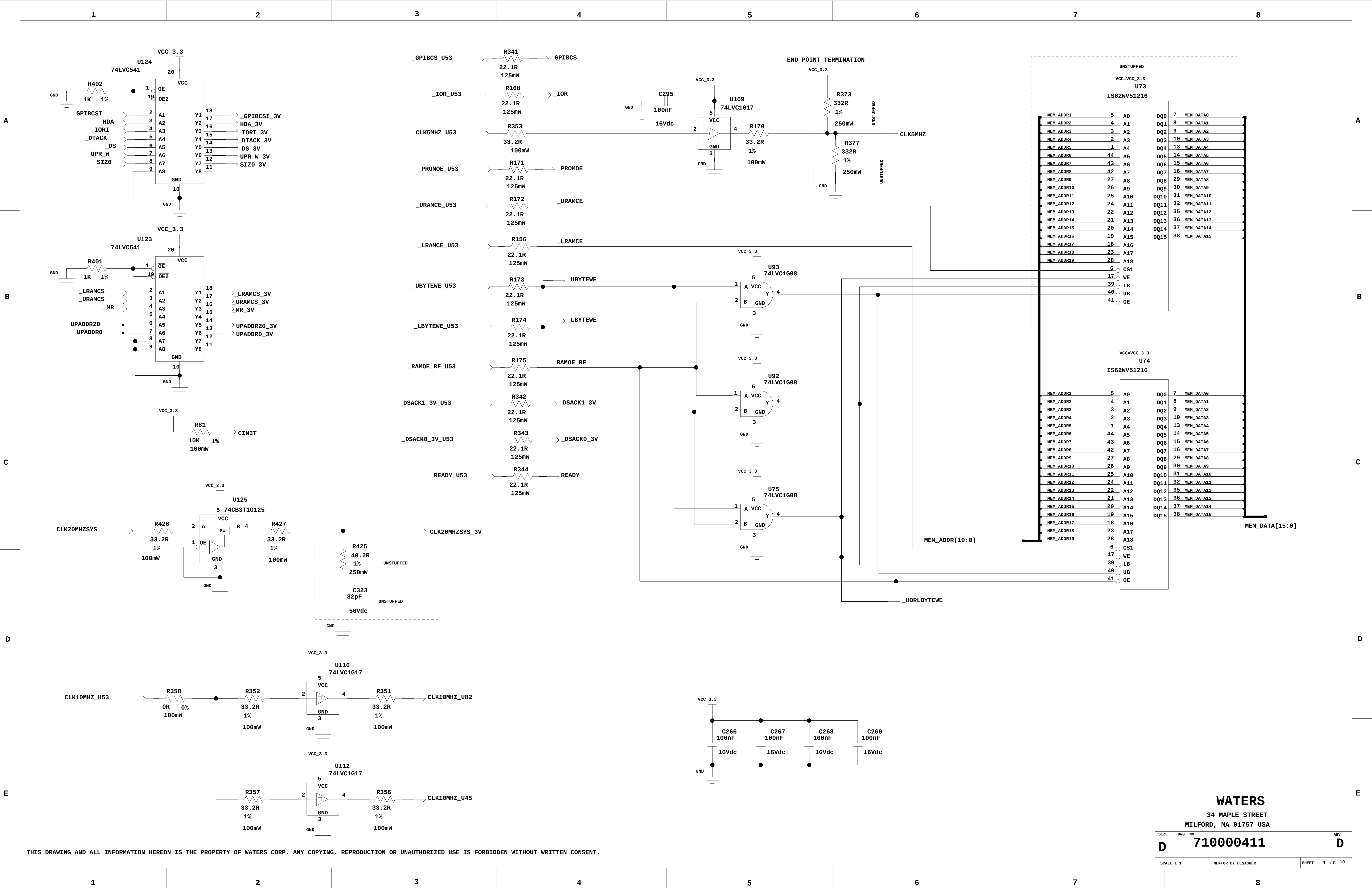
E

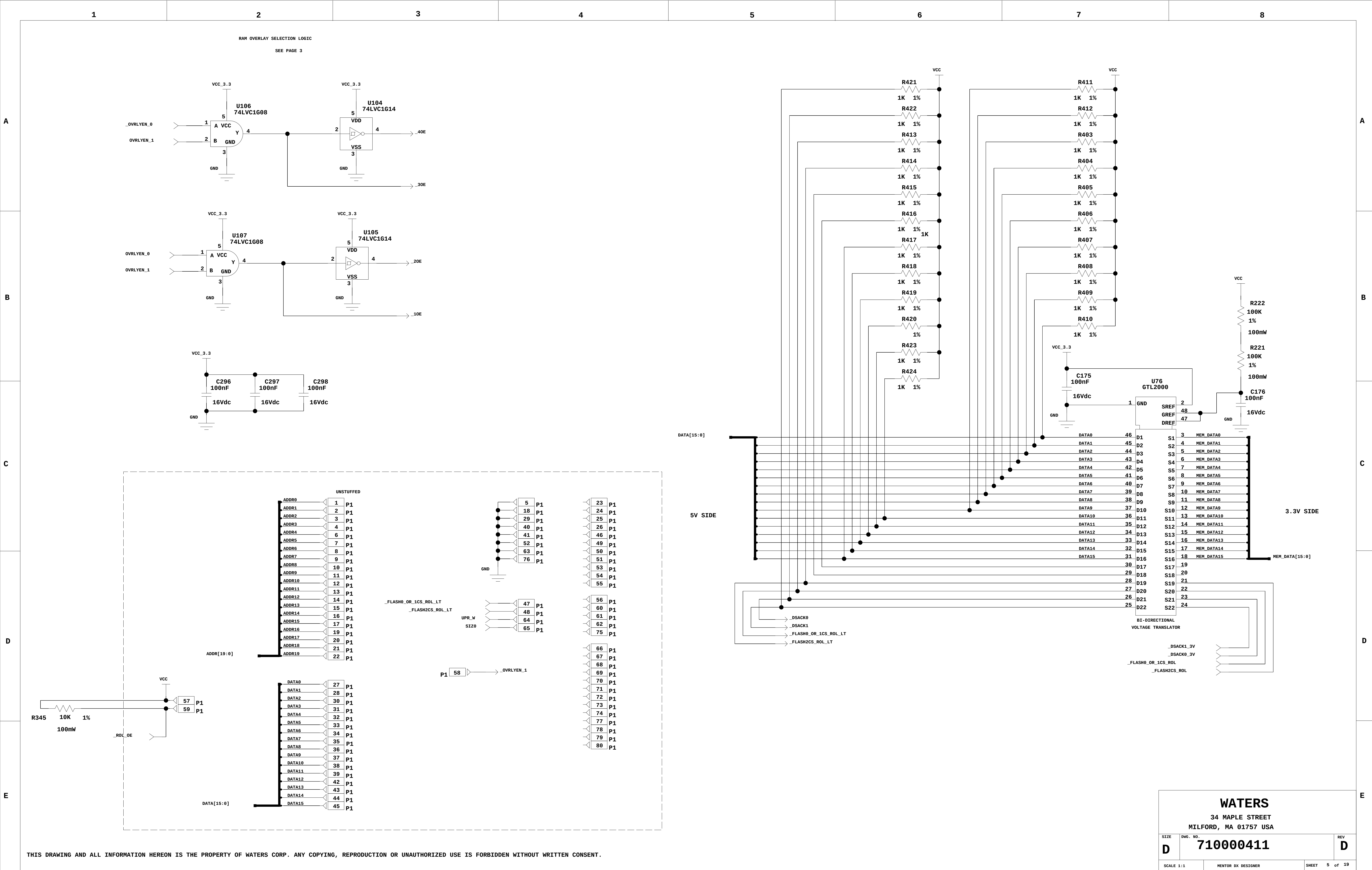


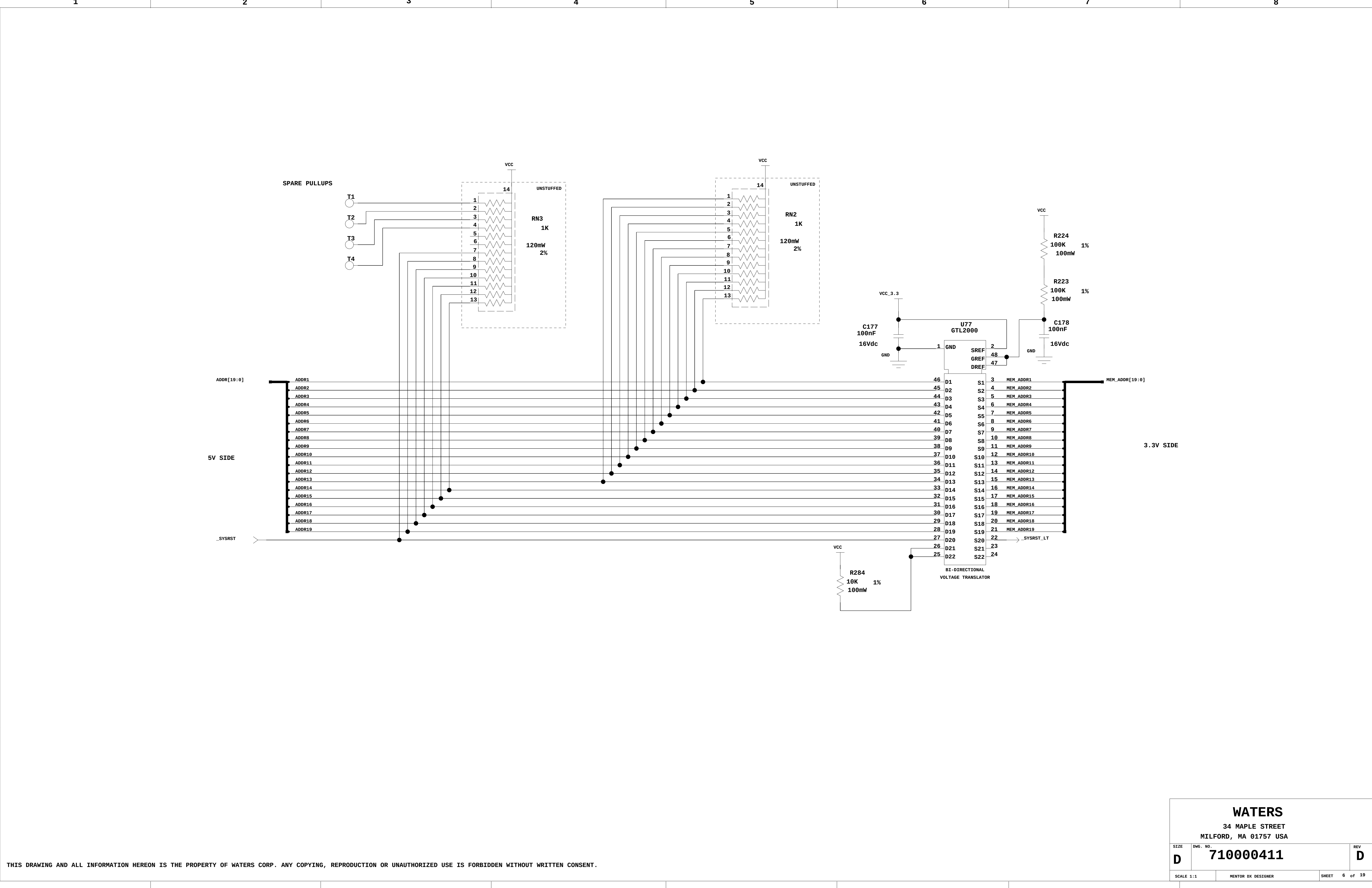
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WATERS		
34 MAPLE STREET		
MILFORD, MA 01757 USA		
SIZE	DWG. NO.	REV
D	710000411	D
SCALE 1:1		SHEET 2 of 19

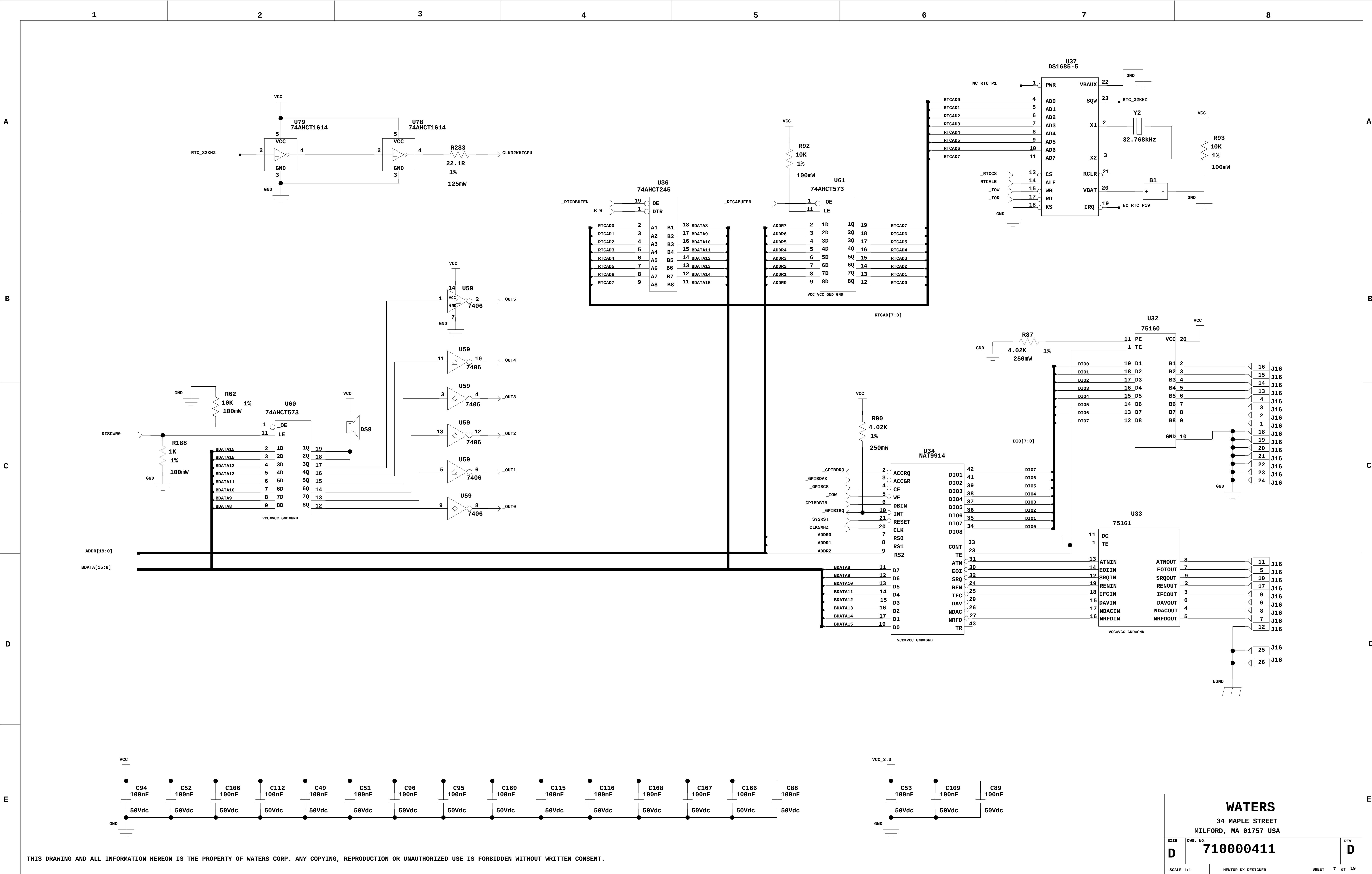








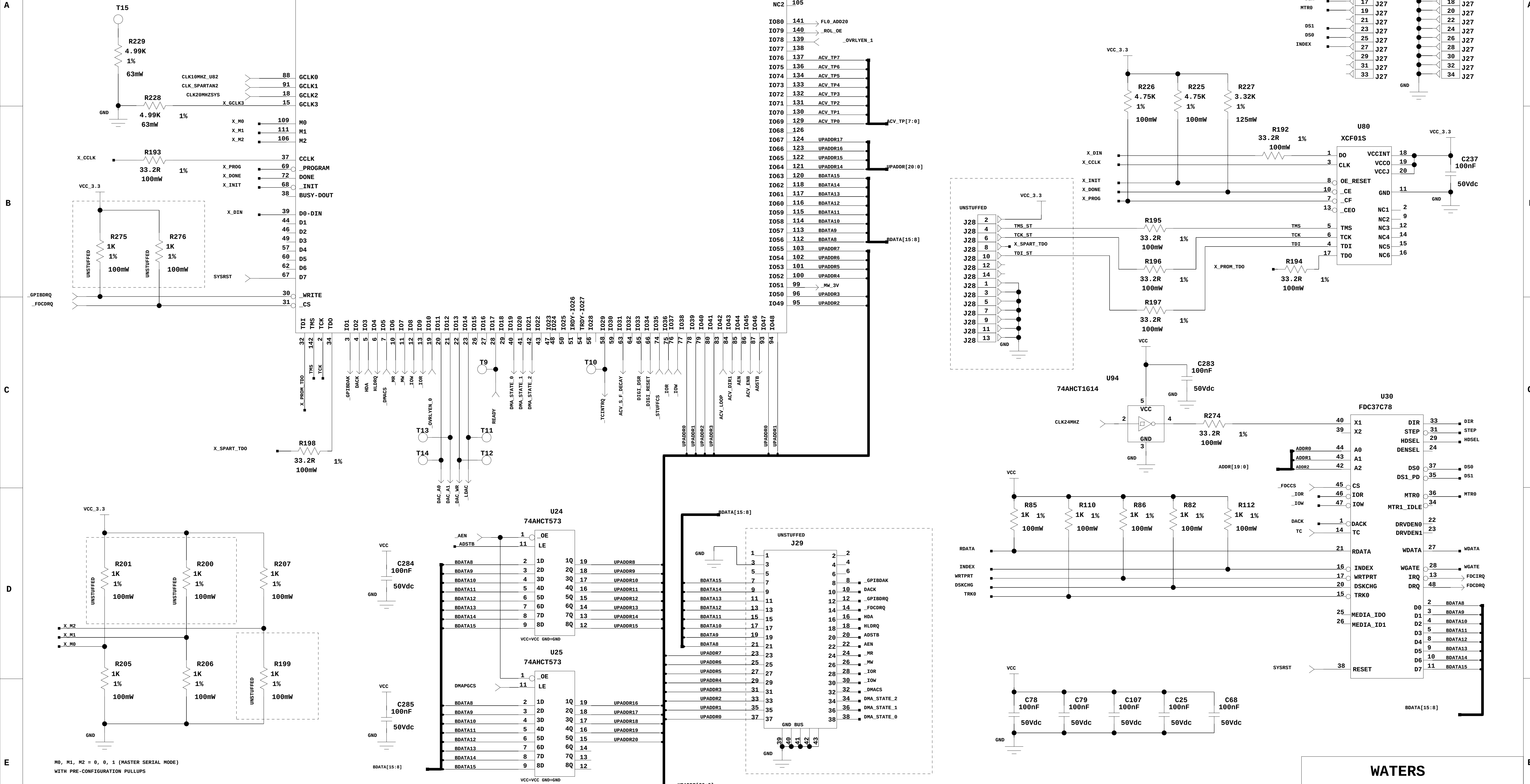
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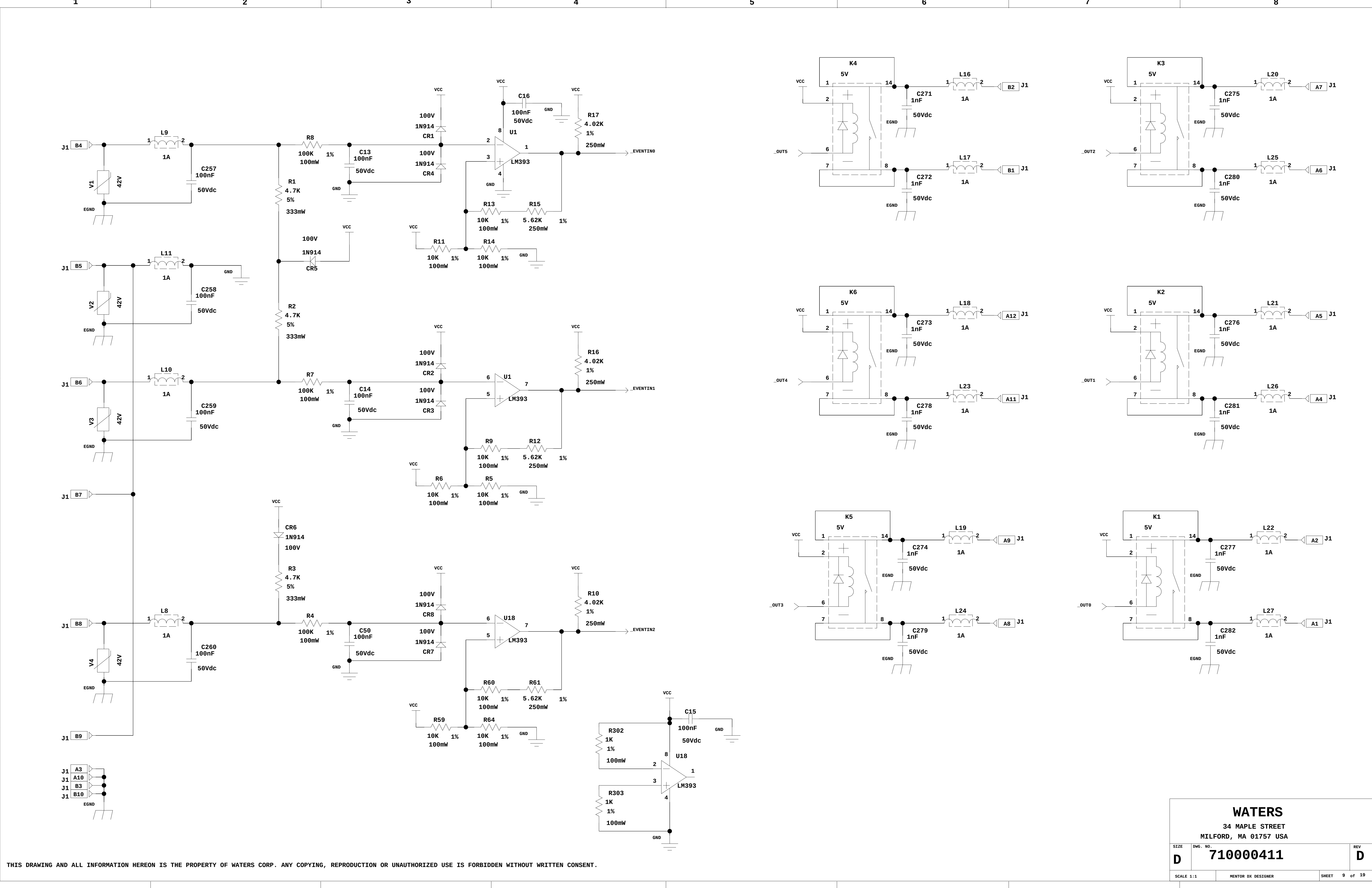
DECOUPLING ON PAGE 19

U82
XC2S50-5TQG144C

VCCINT=VCC_2.5 VCCIO=VCC_3.3

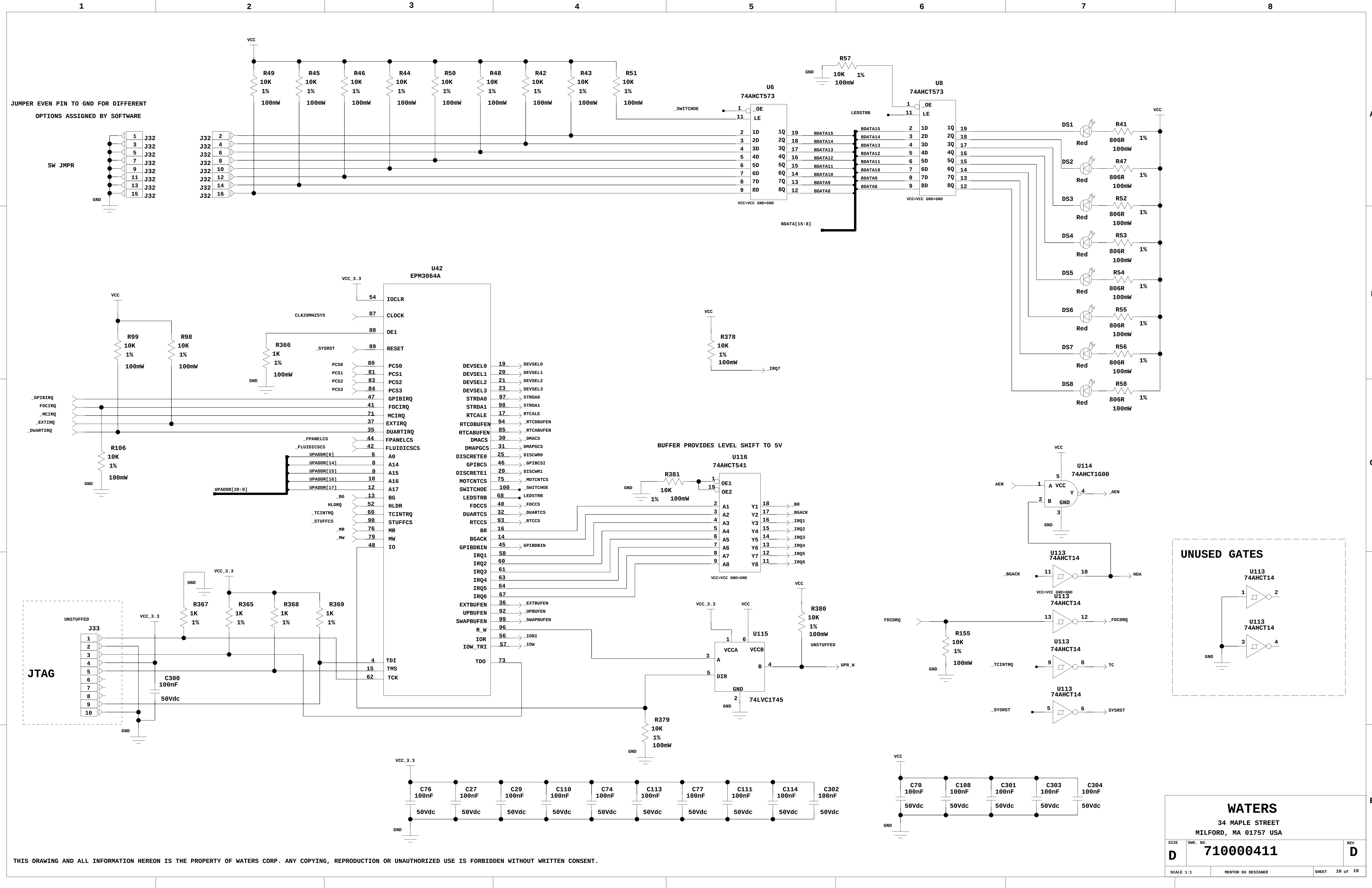


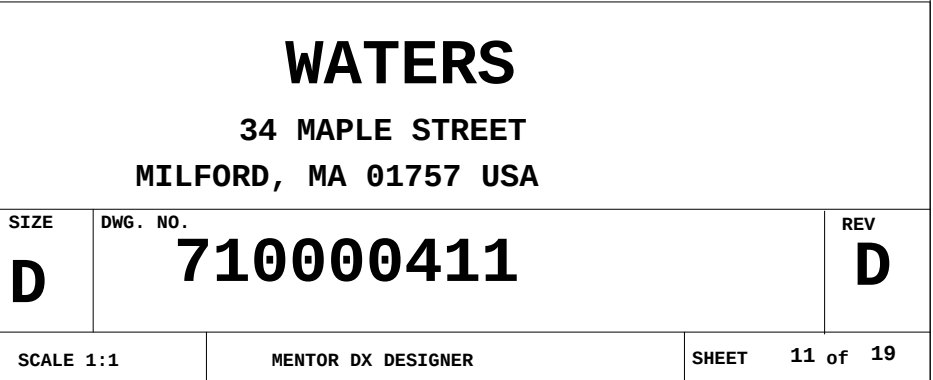
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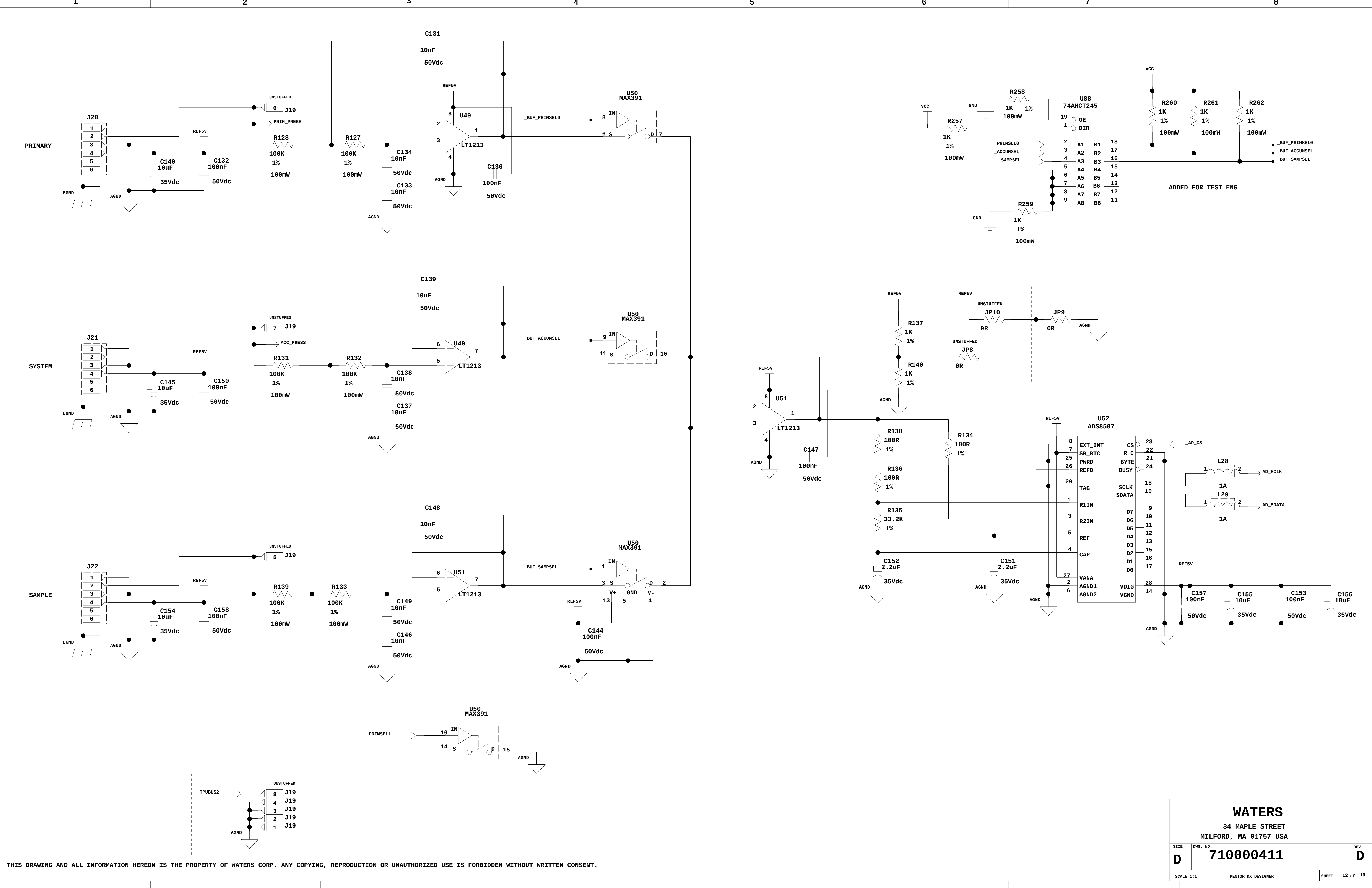


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WATERS		
34 MAPLE STREET		
MILFORD, MA 01757 USA		
SIZE	DWG. NO.	REV
D	710000411	D
SCALE 1:1		SHEET 9 of 19







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WATERS

34 MAPLE STREET

MILFORD, MA 01757 USA

SIZE

D

DWG. NO.

710000411

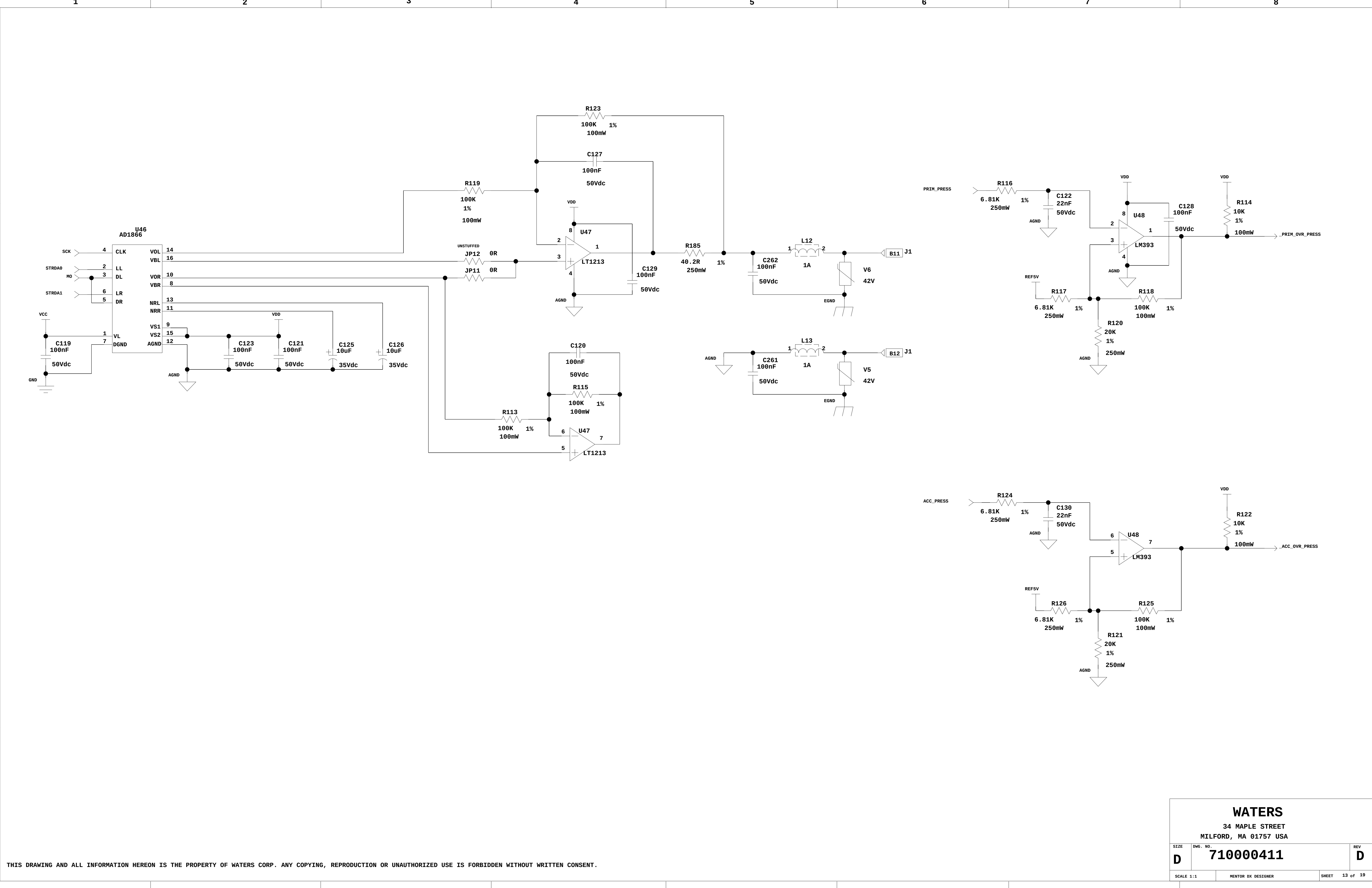
REV

D

SCALE 1:1

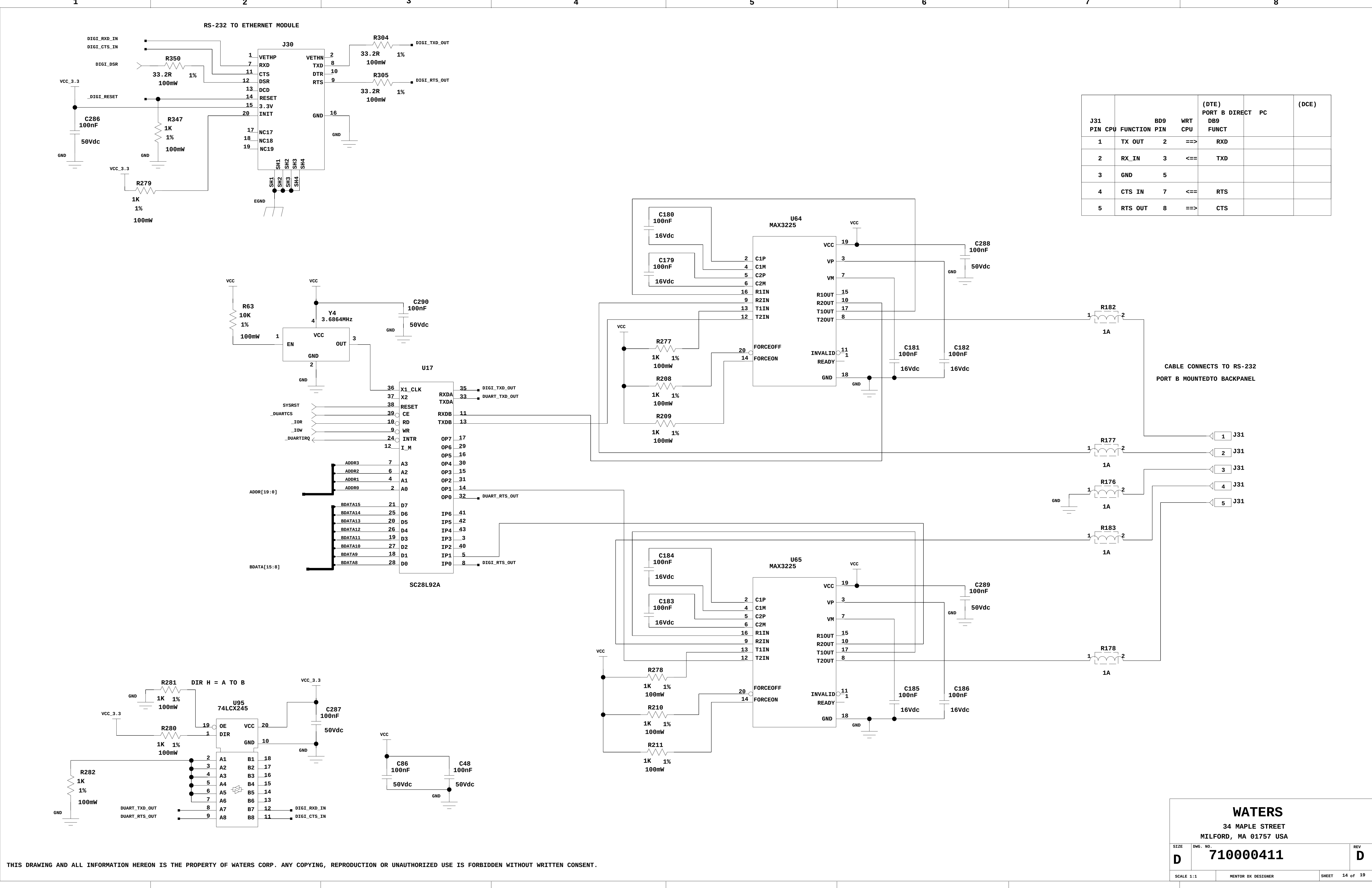
MENTOR DX DESIGNER

SHEET 12 of 19

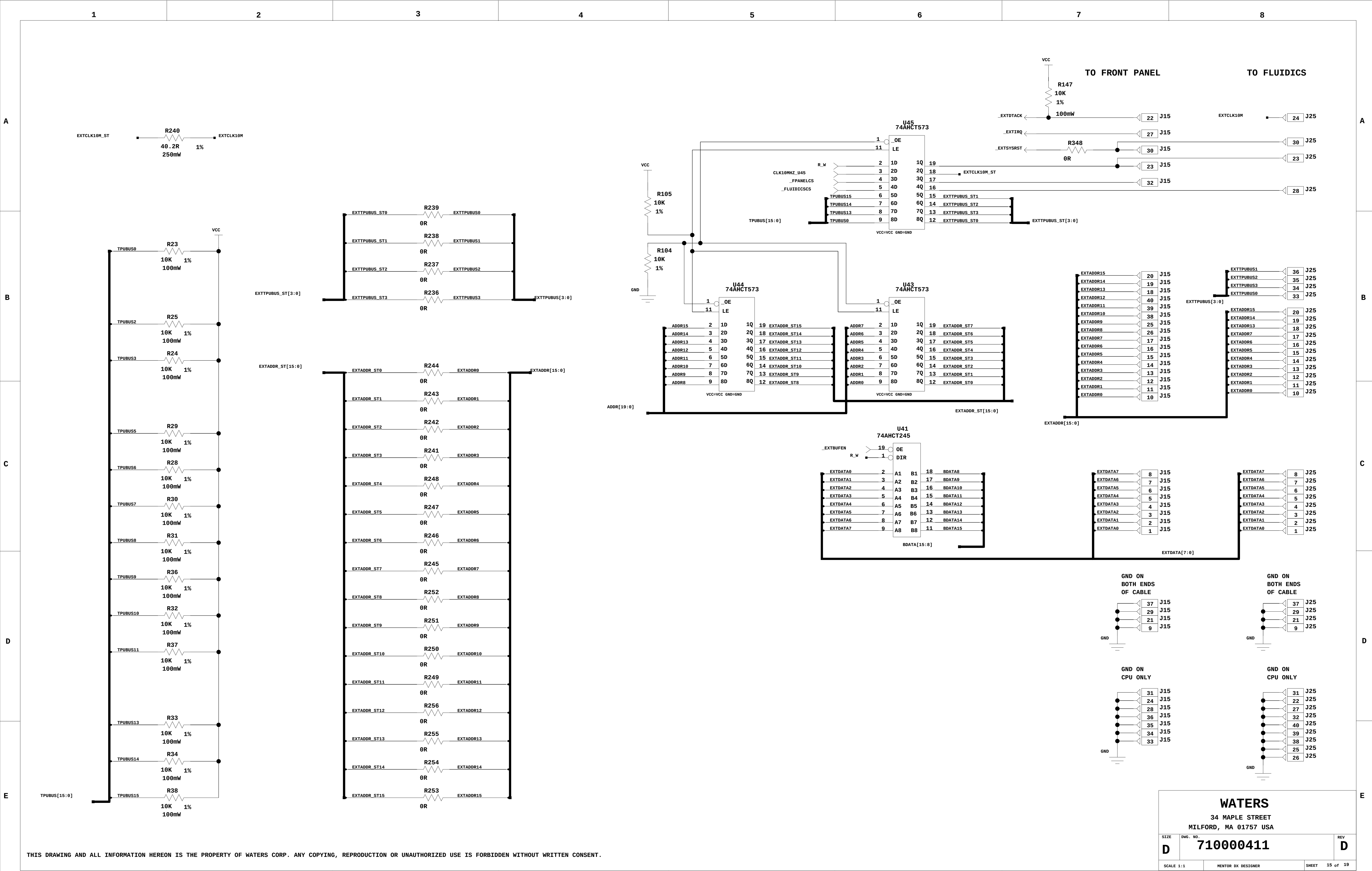


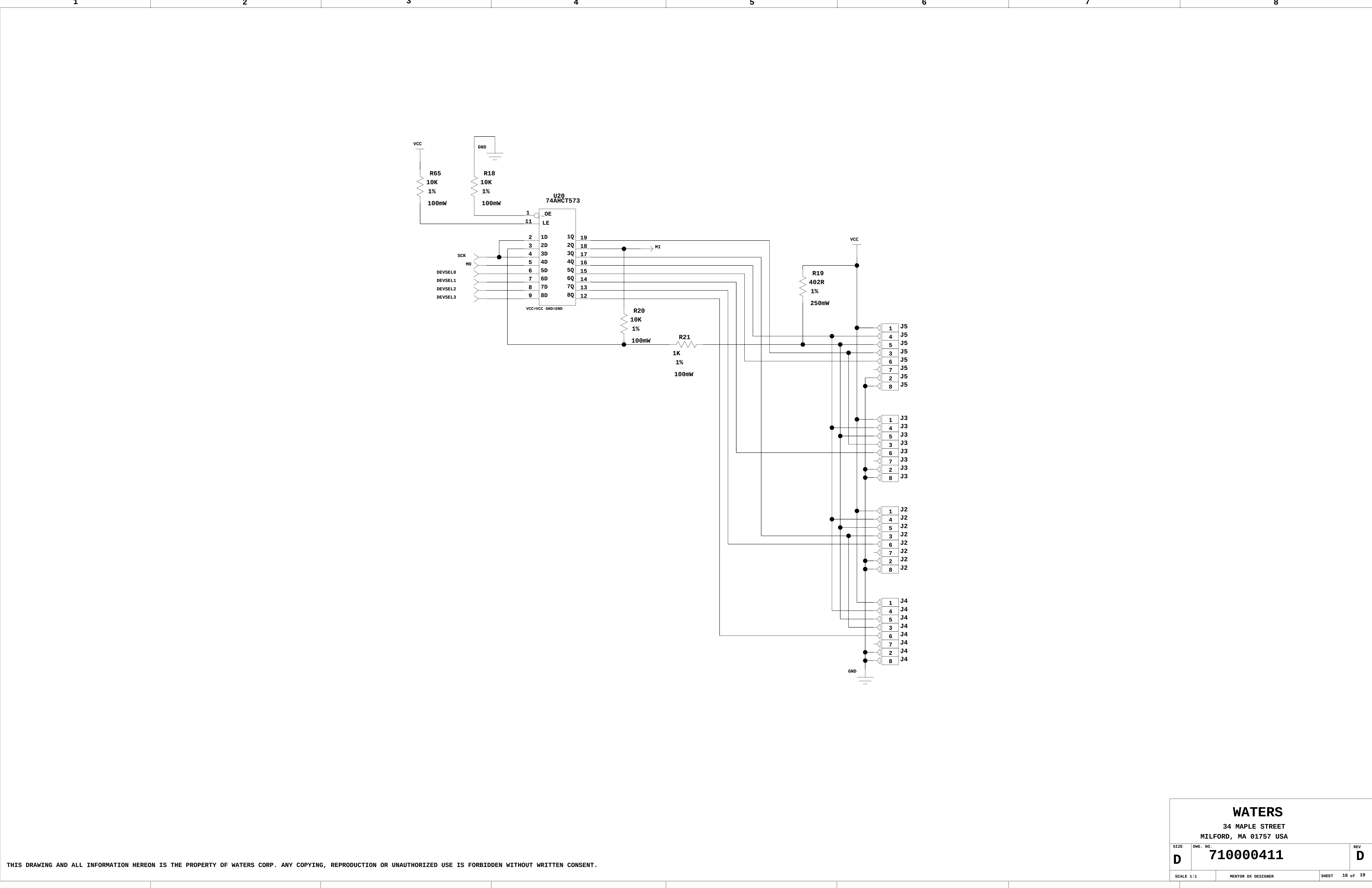
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WATERS 34 MAPLE STREET MILFORD, MA 01757 USA		
SIZE D	DWG. NO. 710000411	REV D
SCALE 1:1		SHEET 13 of 19



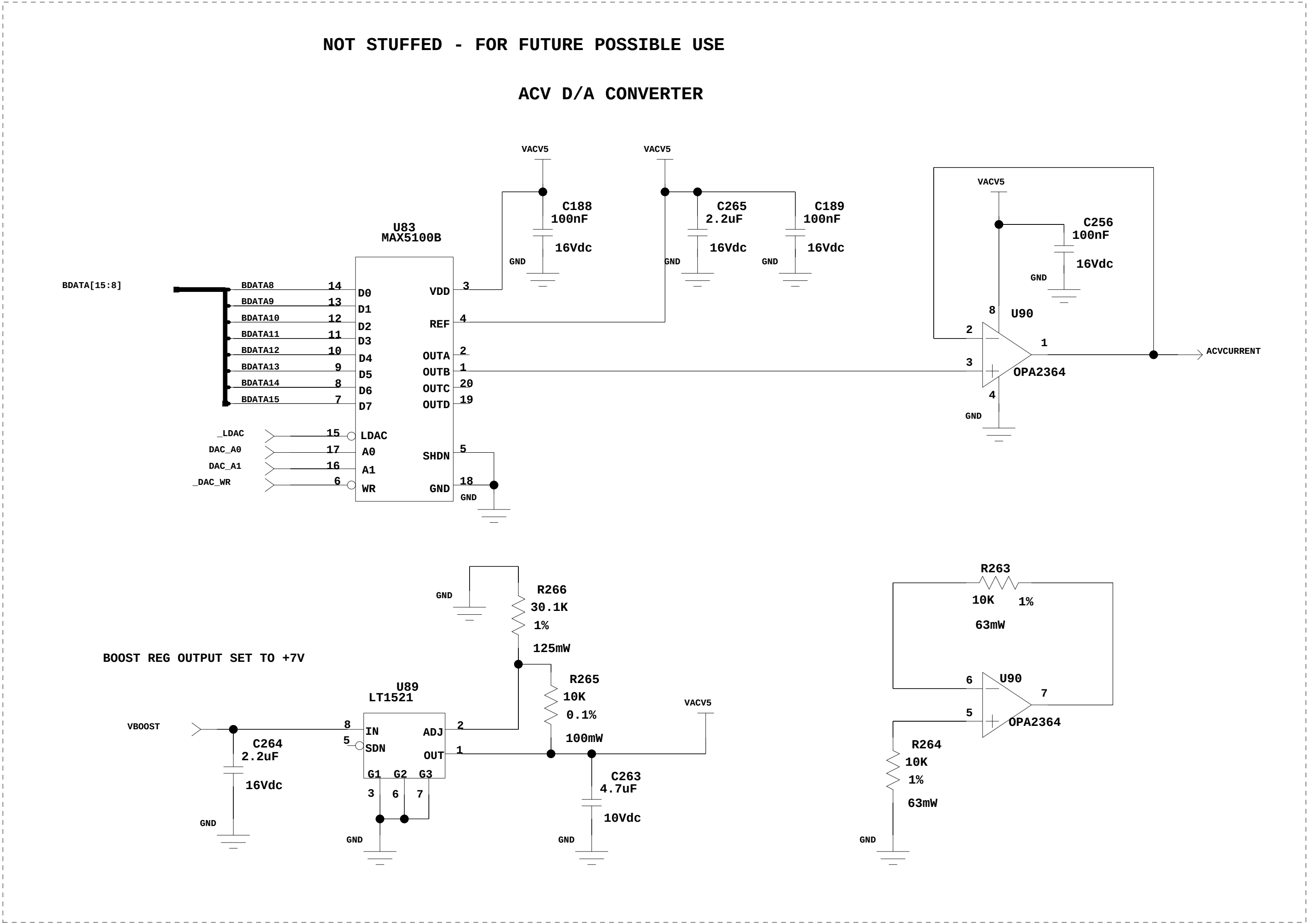
J31 PIN	CPU FUNCTION	BD9 PIN	WRT CPU	(DTE) PORT B DIRECT DB9 FUNCT	PC	(DCE)
1	TX_OUT	2	==>	RXD		
2	RX_IN	3	<==	TXD		
3	GND	5				
4	CTS_IN	7	<==	RTS		
5	RTS_OUT	8	==>	CTS		

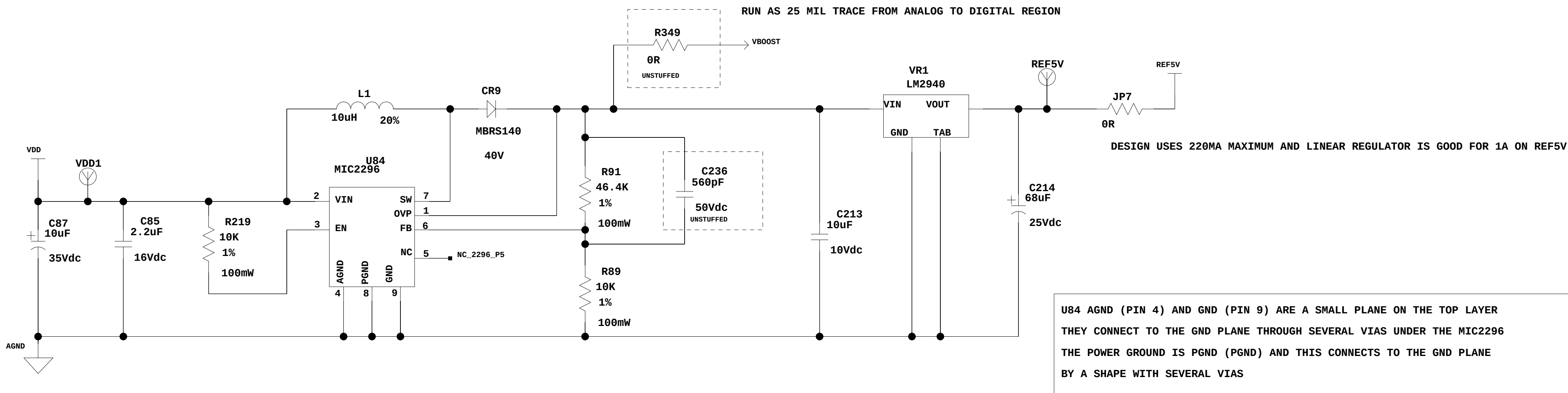
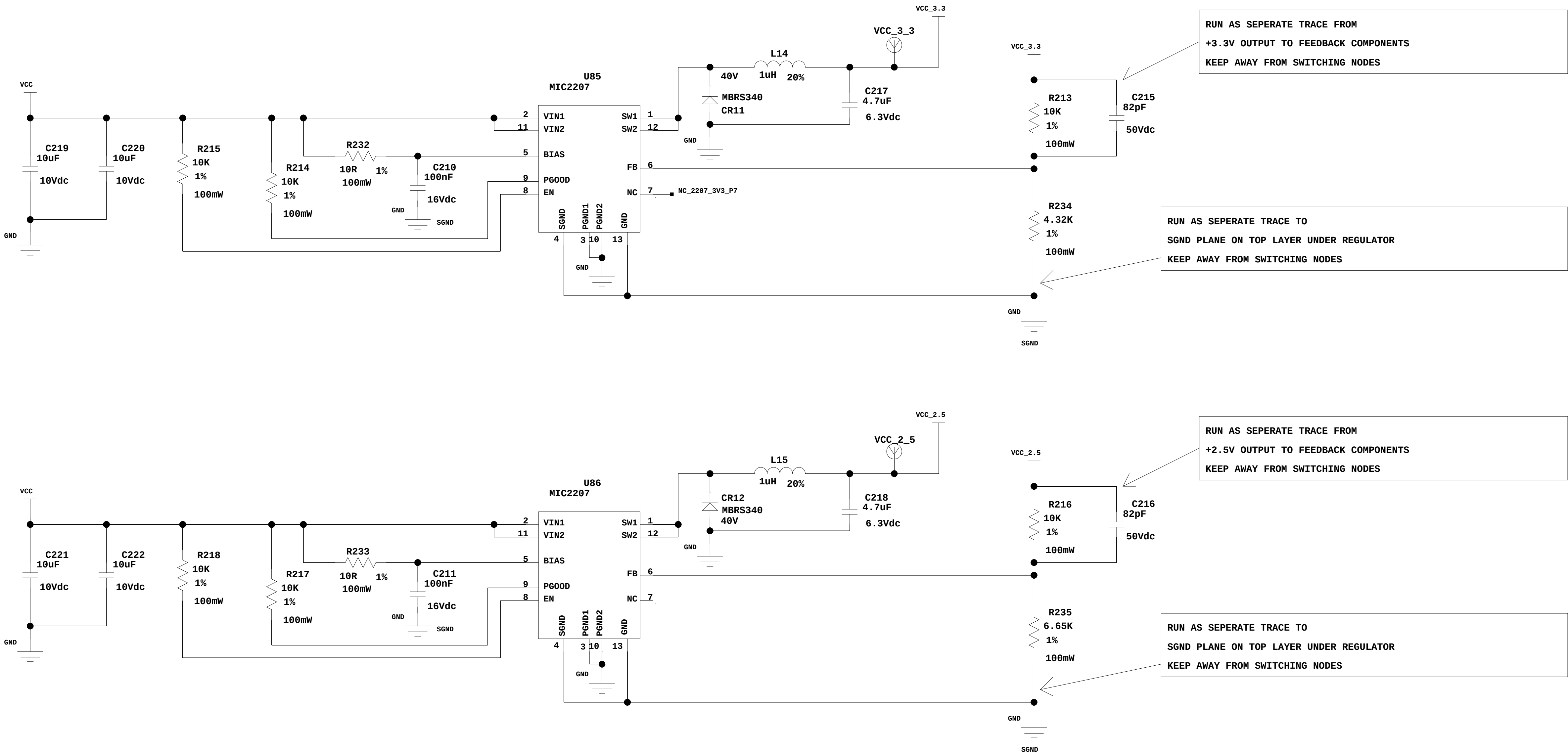


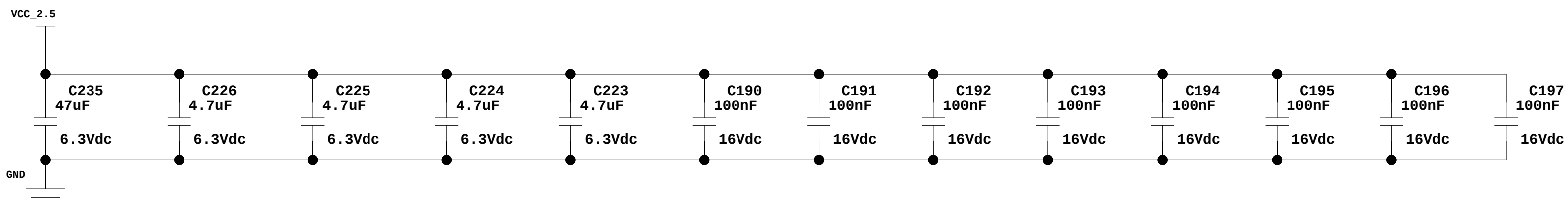


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WATERS		
34 MAPLE STREET		
MILFORD, MA 01757 USA		
SIZE	DWG. NO.	REV
D	710000411	D
SCALE 1:1		SHEET 16 of 19

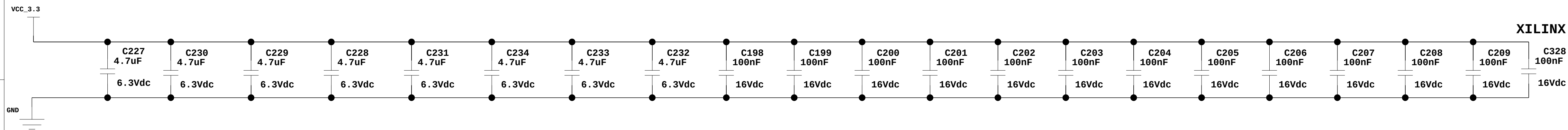






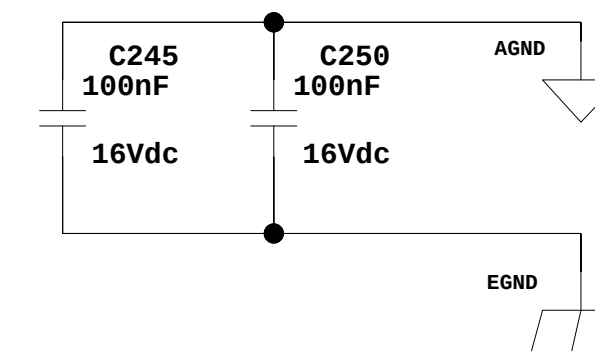
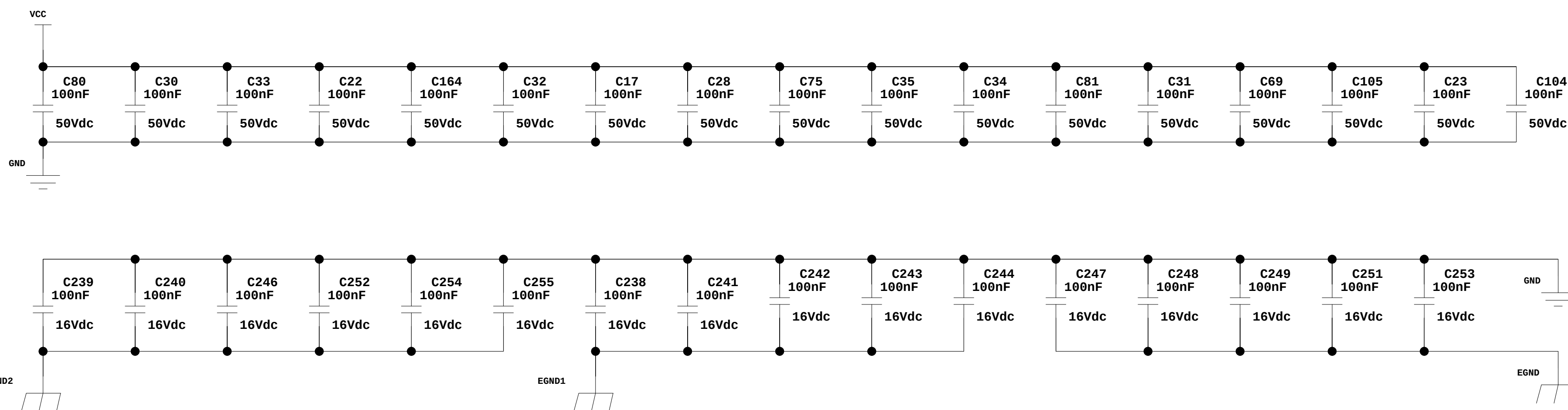
XILINX DECOUPLING RECOMMENDATIONS

ONE 0.1uF CAP PER VCCINT PIN (8 TOTAL)
ONE 4.7uF CAP PER SIDE (4 TOTAL)
ONE 47 uF CAP PER CHIP (1 TOTAL)



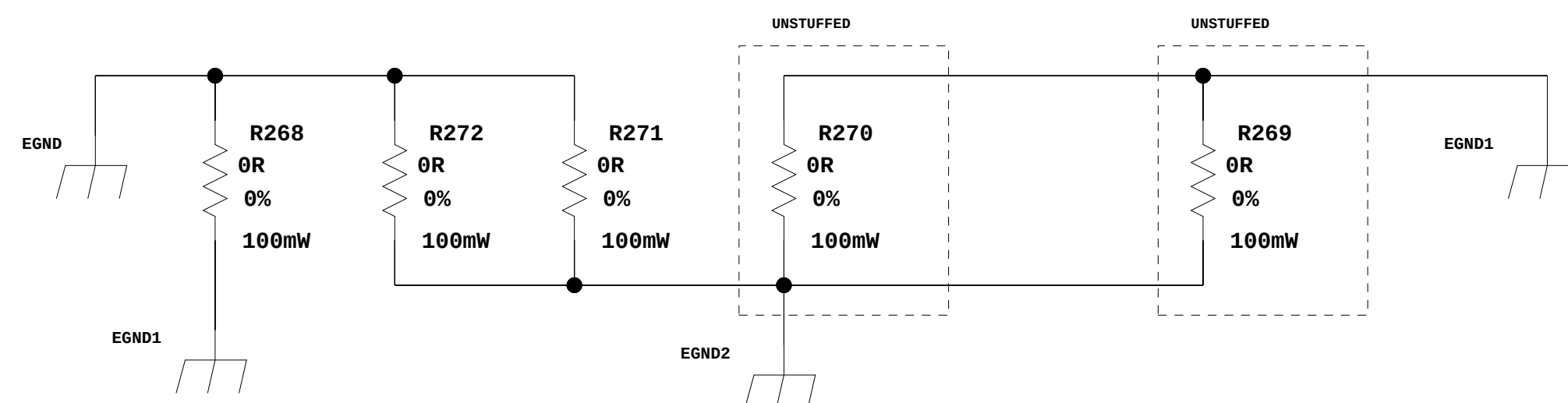
XILINX DECOUPLING RECOMMENDATIONS

ONE 0.1uF CAP PER VCCINT PIN (12 TOTAL)
ONE 4.7uF CAP PER SIDE (8 TOTAL)



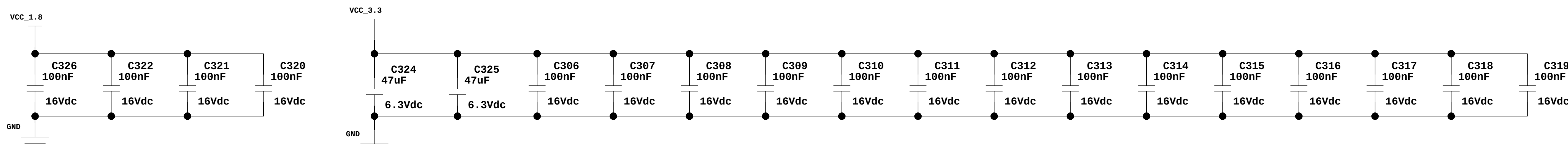
DYNAMIC GND CONNECTION BETWEEN CHASSIS AND DIGITAL GND

GIVES ESD ENERGY ON DIGITAL GND A PATH TO CHASSIS GND



DECOUPLING FOR U53 ON SHEET 11

BULK CAPACITOR TO BE PLACED CLOSE TO U53, BYPASS CAP < 1 cm FROM EACH POWER PIN



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