

Waters THE SCIENCE OF WHAT'S POSSIBLE.™		Equipment Design Verification Report	
Report No: TE0084037-EDVR		Iteration No: 01	SAP No: TE0084037QX

EQUIPMENT DESIGN VERIFICATION REPORT
For the Charge Amp PCB Assembly Test Fixture (TE0084037)

PREPARED BY

Name	Role	Signature	Date
Emma Pierce	Test Validation Engineer		23 Mar 2018

REVIEWED BY

Name	Role	Signature	Date
Rick Davis	Principal Test Engineer		23 MAR 2018

APPROVED BY

Name	Role	Signature	Date
Andre Kopoyan	Senior Operations Quality Engineer		23 Mar 2018

The "Prepared By" signature denotes that this document accurately describes the qualification activities.

The "Reviewed By" signature[s] denotes agreement with the description of the qualification activities.

The "Approved By" signature denotes that this document has been reviewed and approved for overall quality and completeness.

REVISION HISTORY

Iteration	Author	Summary of change
00	Emma Pierce	First document for approval
01	Emma Pierce	Part Number Add

1.0 Purpose

The Charge Amp PCB Assembly Test Fixture (TE0084037) is located in the TE laboratory in Milford, MA. The station is used to perform functional testing of the Charge Amp PCBs of the following part numbers: 210001164 and 210001203. During the test, the UUT is connected and the test program on the GTS is launched. The automated test begins once the UUT serial number has been entered and the electrical performance of the board is verified. Tests include UUT and onboard power, initialization, NVM, voltage clamp, charge amp speed, linearity, and noise. Upon completion, a Final Test Record is automatically generated and saved to the SigmaSure Database.

2.0 Scope of Report

This Equipment Design Verification Report details the verification activities undertaken for the Charge Amp PCB Assembly Test Fixture (TE0084037) based on the requirements of the Validation Assessment Form TE0084037-05FEB2018-VAF which can be found in the TE0084037QX directory of SAP and the EDV Protocol TE0084037-EDV Iteration 01 which can be found in the TE0084037QA directory of SAP.

This Equipment Design Verification Report defines the documents used to verify the Charge Amp PCB Assembly Test Fixture (TE0084037).

3.0 Summary of Results - Statement of Fitness for Intended Use

The Charge Amp PCB Assembly Test Fixture was tested in accordance with the TE0084037-EDV Iteration 01. All required Test Scripts were performed, all objective evidence requirements have been met, and all deviations have been resolved.

Waters now has the necessary documentation in place to ensure that the Charge Amp PCB Assembly Test Fixture complies with Waters' requirements, the latest relevant quality system regulations, and cGMP practices.

Following the approval of this Verification Report, the Charge Amp PCB Assembly Test Fixture (TE0084037) can be considered fully verified and fit for intended use.

4.0 Glossary

The following definitions are used in this document:

Term	Explanation
2p5	2.5 V
A	Amps
AGND	Analog Ground
CA	Charge Amp
cGMP	Current Good Manufacturing Practice
CHx	Channel (x denotes which channel)
EDV(R)	Equipment Design Verification (Report)
EDV(R)	Equipment Design Verification (Report)
FS	Full Scale
GELE	Greater than or Equal to Less than or Equal to (comparison type in TestSequence)
GND	Ground
GTS	Global Test System (multifunctional generic PCB functional test system)
LEGE	Less than or Equal to Greater than or Equal to (comparison type in TestSequence)

Term	Explanation
N	Negative
ns	Nanoseconds
NVM	Non-Volatile Memory
P	Positive
PCB	Printed Circuit Board
PDA	Photodiode Array
PIX	Pixel
PSx	Power Supply (x denotes which power supply)
RMT	Remote
SAP	Enterprise Resource Planning (ERP) software
Sat	Saturated
SN	Serial Number
TSP	Test Specification and Procedure
UI	User Interface
UUT	Unit Under Test
V	Volts
VB	Voltage Bias
VCC	Integrated Circuit Power Supply Voltage
VREF	Reference Voltage
x	Test Variable
Ω	Ohm
§	Section

5.0 Training

The executor of this verification is the author of TE0084037-EDV Iteration 01 and is considered trained to the protocol. The executor of this verification has been trained to the Waters GTS Operation TSP 735002109, Ver. 00 and to the 210001203 Output Specification 721015389, Ver. 00 and has been given hands on GTS training by the system owner. The training records are provided as Attachment 7.1

6.0 Verification Results

6.1 Test Script EDV-01: Specification and Functional Verification and Test Script EDV-02: Fault Insertion were not performed as part of this verification because P/N: 210001164 is not being changed.

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6.2 Test Script EDV-03: Specification and Functional Verification was performed according to TE0084037-EDV Iteration 01. The completed Test Script Data Sheet is provided as Attachment 7.2.

6.2.1 It was verified that testing a known good unit of Part #210001203 resulted in the test system identifying the unit as passing. This test was performed using the Charge Amp PCB Assembly Test Fixture (TE0084037) on the GTS platform (TE82988-1). The passing test record printed from the SigmaSure Database has been provided as Attachment 7.3.

6.3 Test Script EDV-04: Fault Insertion Test was performed according to TE0084037-EDV Iteration 01. The completed Test Script Data Sheet is provided as Attachment 7.4.

6.3.1 Test UUT Power (Measure PS1 (+5) Voltage)

A 2 Ω resistor was connected across the VCC and GND test points before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing result is shown below:

Measure PS1 (+5V) voltage	
Status:	Failed
Numeric:	3.194
Units:	V
Limits:	
Low:	4.8
High:	5.2
Comp:	GELE
Module Time:	0.3151267

6.3.2 Test UUT Power (Measure PS1 (+5) Current)

A 16 Ω resistor was connected across the VCC and GND test points before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing result is shown below:

Measure PS1 (+5V) Current	
Status:	Failed
Numeric:	1.221
Units:	A
Limits:	
Low:	0.800
High:	1.200
Comp:	GELE
Module Time:	0.1337273

6.3.3 Test UUT Power (Measure PS3 (-15) Voltage)

A 25 Ω resistor was connected across the N15V and AGND test points before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing result is shown below:

Measure PS3 (-15V) Voltage	
Status:	Failed
Numeric:	0.029
Units:	V
Limits:	
Low:	14.7
High:	15.3
Comp:	GELE
Module Time:	0.2668166

6.3.4 Test UUT Power (Measure PS3 (-15) Current)

A 200 Ω resistor was connected across the N15V and AGND test points before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing result is shown below:

Measure PS3 (-15V) Current	
Status:	Failed
Numeric:	0.126
Units:	A
Limits:	
Low:	0.000
High:	0.100
Comp:	GELE
Module Time:	0.1064322

6.3.5 Test UUT Power (Measure PS4 (+15) Voltage)

A 25 Ω resistor was connected across the P15V and AGND test points before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing result is shown below:

Measure PS4 (+15V) Voltage	
Status:	Failed
Numeric:	3.534
Units:	V
Limits:	
Low:	14.7
High:	15.3
Comp:	GELE
Module Time:	0.367114

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6.3.6 Test UUT Power (Measure PS4 (+15V) Current)

A 200 Ω resistor was connected across the P15V and AGND test points before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing result is shown below:

Measure PS4 (+15V) Current	
Status:	Failed
Numeric:	0.140
Units:	A
Limits:	
Low:	0.000
High:	0.100
Comp:	GELE
Module Time:	0.1014211

6.3.7 Test Onboard Power (Test 14A)

The 14A probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test 14A	
Status:	Failed
Numeric:	-0.00196158
Units:	V
Limits:	
Low:	13.8
High:	14.2
Comp:	GELE
Module Time:	1.1295795

6.3.8 Test Onboard Power (Test N14A)

The N14A probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test N14A	
Status:	Failed
Numeric:	-0.00157671
Units:	V
Limits:	
Low:	-14.2
High:	-13.8
Comp:	GELE
Module Time:	1.160136

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6.3.9 Test Onboard Power (Test 5A)

The 5A probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test 5A	
Status:	Failed
Numeric:	-0.001695212
Units:	V
Limits:	
Low:	4.6
High:	5.1
Comp:	GELE
Module Time:	1.1672516

6.3.10 Test Onboard Power (Test N5A)

The N5A probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test N5A	
Status:	Failed
Numeric:	-0.001507846
Units:	V
Limits:	
Low:	-5.1
High:	-4.6
Comp:	GELE
Module Time:	1.1633092

6.3.11 Test Onboard Power (Test PDA_VB)

Pin 8 in the PDA socket was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test PDA_VB	
Status:	Failed
Numeric:	-0.002125245
Units:	V
Limits:	
Low:	1.996
High:	2.002
Comp:	GELE
Module Time:	1.161373

6.3.12 Test Onboard Power (Test VREF_2p5)

The VREF_2p5 probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test VREF_2p5	
Status:	Failed
Numeric:	-0.002032577
Units:	V
Limits:	
Low:	2.4
High:	2.6
Comp:	GELE
Module Time:	1.1474885

6.3.13 Test Onboard Power (Test PDA_5A)

Pin 4 in the PDA socket was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test PDA_5A	
Status:	Failed
Numeric:	-0.001823919
Units:	V
Limits:	
Low:	4.8
High:	5.1
Comp:	GELE
Module Time:	1.1533508

6.3.14 Test Onboard Power (Test RMT3.3)

The RMT3.3 probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test RMT3.3	
Status:	Failed
Numeric:	-0.001736311
Units:	V
Limits:	
Low:	3.2
High:	3.4
Comp:	GELE
Module Time:	1.1387561

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6.3.15 Test Onboard Power (Test VCC3.3)

The VCC3.3 probe was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test VCC3.3	
Status:	Failed
Numeric:	-0.001645713
Units:	V
Limits:	
Low:	3.2
High:	3.4
Comp:	GELE
Module Time:	1.1481836

6.3.16 Test Over Voltage Clamp (Set Input Voltage)

The CH1 cable was disconnected from the GTS scope before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test Over-Voltage Clamp	
Status:	Failed
Module Time:	26.8527335

6.3.17 Test Over Voltage Clamp (Test Clamp Pulse Width)

A breakpoint was inserted at the "Test V_Sat Pulse Width" step in the "Clamping" sequence. When the test reached the breakpoint the CH1 cable was disconnected from the GTS scope and the system was triggered using the "Force Trigger" button on the scope before continuing the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test V_Sat Pulse Width	
Status:	Failed
Numeric:	4.3422
Units:	ns
Limits:	
Low:	6.2
High:	56.2
Comp:	GELE
Module Time:	0.7085767

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6.3.18 Test Over Voltage Clamp (Test P_PDA Peak Voltage)

The CH2 cable was disconnected from the GTS scope before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test P_PDA Peak Voltage	
Status:	Failed
Numeric:	0.1072107
Units:	V
Limits:	
Low:	4.096
High:	4.5
Comp:	GELE
Module Time:	1.6727667

6.3.19 Test Charge Amp Speed (Signal Rise Time)

A breakpoint was inserted at the "Cfg TDS CH2 Speed" step in the "Charge Amp Speed" sequence (refer to § 8.1). When the test reached the breakpoint the CH2 cable was disconnected from the GTS scope and the system was triggered using the "Force Trigger" button on the front of the scope before continuing the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Signal Rise Time	
Status:	Failed
Numeric:	4976.9
Units:	ns
Limits:	
Low:	30
High:	150
Comp:	GELE
Module Time:	3.9928536

6.3.20 Test Linearity (Slope)

The run modes for the "Test Over-Voltage" and "Test Charge Amp Speed" steps were set to "skip" and pin 9 in the PDA socket was removed before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Slope	
Status:	Failed
Numeric:	0.062738095
Limits:	
Low:	-54000
High:	-49000
Comp:	GELE

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6.3.21 Test Noise (Fixed Noise)

The run mode of the "Vacuum Off" step in the "Fixed Noise" sequence (refer to § 8.1) was set to "skip" before starting the test. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Fixed Noise	
Status:	Failed
Numeric:	9.956055699
Limits:	
Low:	2
High:	7
Comp:	GELE
Module Time:	10.2511164

6.3.22 Test NVM (Test NVM)

A breakpoint was inserted at the "Test NVM" step in the main sequence. When the test reached the breakpoint the ribbon cable on the test fixture was removed and the test sequence was continued. The test step failed, indicating the test system correctly identified the fault. A screen capture of the failing results is shown below:

Test NVM	
Status:	Failed
Module Time:	15.3464375
NVM Device Read Error	

6.4 This table provides a summary of each test script as performed according to TE0084037-EDV Iteration 01 along with the attachment location of all objective evidence. The table also indicates any deviation taken from the scripts during qualification.

Script or Section	Pass/Fail	Objective Evidence	Deviations
EDV-01	Pass	Attachments 7.2 and 7.3	None
EDV-02	Pass	Attachment 7.4	Two: see § 8.0

7.0 Attachments

- 7.1 Completed Executor Training Record
- 7.2 Completed Test Script EDV-01: Specification and Functional Verification
- 7.3 Objective Evidence EDV-01: Passing Test Record for P/N: 210001203 (S/N: 261217023M)
- 7.4 Completed Test Script EDV-02: Fault Insertion

8.0 Deviation from Test Equipment Qualification

There were two deviations generated during the execution of the TE0084037-EDV Iteration 01.

8.1 Description: The test step and test sequence names listed in Step 4.1 of Test Script EDV-04: Fault Insertion are incorrect. The fault insertion method should be:

Insert a breakpoint at the "Cfg TDS CH2 Speed" step in the "Charge Amp Speed" test sequence. When the test reaches the breakpoint disconnect the scope CH2 cable, push the "Force Trigger" button on the front panel of the scope, then continue.

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8.1.1 Proposed Corrective Action: This deviation is the result of a protocol error. No corrective action was necessary.

8.1.2 Resolution: The fault insertion was completed as described in § 6.3.19 of this report. The EDV Protocol will be updated to correct this error.

8.2 Description: The test sequence name listed in Step 6.1 of Test Script EDV-04: Fault Insertion is incorrect. The fault insertion method should be:

Change the "Vacuum Off" run mode to "Skip" in the "Fixed Noise" sequence before starting the test.

8.2.1 Proposed Corrective Action: This deviation is the result of a protocol error. No corrective action was necessary.

8.2.2 Resolution: The fault insertion was completed as described in § 6.3.21 of this report. The EDV Protocol will be updated to correct this error.

9.0 References

The current approved versions of the following documents are referenced within this report:

Document Number	Document Title
TE0084037-05FEB2018-VAF	Validation Assessment Form for P/N: 210001203 Add
TE0084037-Memo_Iteration 01	Traceability Matrix for Charge Amp PCB Assembly Test Fixture
TE0084037-EDV_Iteration 01	Equipment Design Verification for the Charge Amp PCB Assembly Test Fixture
721015389	210001203 Output Specification
721014067	210001164 Output Specification
730002845	Validation Report Template
735002109, Ver. 00	Waters GTS Operation TSP
735004006, Ver. 00	Waters GTS Preventative Maintenance and Calibration Procedure

Title: individual Training Form

Document No: 730002657

Version No: 00

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Training Type:	Verbal Hands-on Training		
Name:	Emma Pierce	Employee ID¹	034916
Date of Training	15 Sept 2017		
Comments:	N/A		

Document Number	Title	Rev. #
735002109	Waters GTS Operation TSP	00
721014167 entry error 721014067 ECP 26 Oct 2017	210001164 Output Specification	01
N/A	Hands on GTS Training	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A


Test Validation Engineer
26 Oct 2017
 Employee's Signature Title Date


Princ. Test Engineer
26 Oct 2017
 Trainer's Signature Title Date

Document No.: TE0084037-EDVR
 Iteration No.: 01
 Attachment: 7.1 Page: 1 of 2

¹ Without preceding "90"

Title: individual Training Form

Document No: 730002657

Version No: 00

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Training Type:	Read and Understood		
Name:	Emma Pierce	Employee ID¹	034916
Date of Training	14 March 2018		
Comments:	N/A		

Document Number	Title	Rev. #
721015389	210001203 Output Specification	00
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A
N/A	N/A	N/A

	<u>Test Validation Engineer</u>	<u>14 March 2018</u>
Employee's Signature	Title	Date
<u>N/A self training per 14 Mar 2018</u>		
Trainer's Signature	Title	Date

Document No.: TE00841037-EDVR
Iteration No.: 01
Attachment: 7.1 Page: 2 of 2

¹ Without preceding "90"

Report No: TE0084037-EDV

Iteration No: 01

SAP No: TE0084037QA

Test Name: Specification and Functional Verification

Test Script No.: EDV-03

Equipment Number: TE0084037

Equipment Name: Charge Amp PCB Assembly Test Fixture

Software Version: A

Part Number: 210001203

Serial Number: 261217023M

Purpose:

To ensure that obtained results that are within specification are measured/reported as such by the system. To ensure that critical to quality specifications are properly implemented for test.

Test execution:

Perform the Test Script steps in order to verify system specifications and functionality.

Run the equipment until completion. Verify that all acceptance criteria listed below are met and documented on the Final Test Record.

Objective evidence:

Completed Test Script Data Sheet

Copy of the Final Test record(s) for each UUT

Description Specification	Acceptance Criteria	Actual Result	Pass / Fail	Initial & Date
1. Test Fixture ID	PASS	PASS	Pass	EUP 14 Mar 2018
1.1. Test Fixture ID	4	4	Pass	EUP 14 Mar 2018
2. Fixture Down Detect	PASS	PASS	Pass	EUP 14 Mar 2018
3. Test UUT Power	PASS	PASS	Pass	EUP 14 Mar 2018
3.1. Measure PS1 (+5) Voltage	LSL: 4.8 V USL: 5.2 V	5 V	Pass	EUP 14 Mar 2018
3.2. Measure PS1 (+5) Current	LSL: 0.8 A USL: 1.2 A	0.944 A	Pass	EUP 14 Mar 2018
3.3. Measure PS3 (-15) Voltage	LSL: 14.7 V USL: 15.3 V	15.005 V	Pass	EUP 14 Mar 2018
3.4. Measure PS3 (-15) Current	LSL: 0 A USL: 0.1 A	0.05 A	Pass	EUP 14 Mar 2018
3.5. Measure PS4 (+15) Voltage	LSL: 14.7 V USL: 15.3 V	15.002 V	Pass	EUP 14 Mar 2018
3.6. Measure PS4 (+15) Current	LSL: 0 A USL: 0.1 A	0.064 A	Pass	EUP 14 Mar 2018
4. Report Text	PASS	PASS	Pass	EUP 14 Mar 2018
4.1. Report Text	Unprogrammed	Unprogrammed	Pass	EUP 14 Mar 2018
5. Write Flash Memory	PASS	PASS	Pass	EUP 14 Mar 2018
6. Test UUT Power	PASS	PASS	Pass	EUP 14 Mar 2018
6.1. Measure PS1 (+5) Voltage	LSL: 4.8 V USL: 5.2 V	5 V	Pass	EUP 14 Mar 2018
6.2. Measure PS1 (+5) Current	LSL: 0.8 A USL: 1.2 A	0.918 A	Pass	EUP 14 Mar 2018

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6.3. Measure PS3 (-15) Voltage	LSL: 14.7 V USL: 15.3 V	15.005 V	Pass	Eep 14 Mar 2018
6.4. Measure PS3 (-15) Current	LSL: 0 A USL: 0.1 A	0.054	Pass	Eep 14 Mar 2018
6.5. Measure PS4 (+15) Voltage	LSL: 14.7 V USL: 15.3 V	15.002 V	Pass	Eep 14 Mar 2018
6.6. Measure PS4 (+15) Current	LSL: 0 A USL: 0.1 A	0.065 A	Pass	Eep 14 Mar 2018
7. Initialize	PASS	PASS	Pass	Eep 14 Mar 2018
8. Test Onboard Power Supplies	PASS	PASS	Pass	Eep 14 Mar 2018
8.1. Test 14A	LSL: 13.8 V USL: 14.2 V	13.932871577 V	Pass	Eep 14 Mar 2018
8.2. Test N14A	LSL: -14.2 V USL: -13.8 V	-13.978155865 V	Pass	Eep 14 Mar 2018
8.3. Test 5A	LSL: 4.8 V USL: 5.1 V	5.015622946 V	Pass	Eep 14 Mar 2018
8.4. Test N5A	LSL: -5.1 V USL: -4.8 V	-5.033734571 V	Pass	Eep 14 Mar 2018
8.5. Test PDA_VB	LSL: 1.998 V USL: 2.002 V	1.999611215 V	Pass	Eep 14 Mar 2018
8.6. Test VREF_2p5	LSL: 2.4 V USL: 2.6 V	2.499649048 V	Pass	Eep 14 Mar 2018
8.7. Test PDA_5A	LSL: 4.8 V USL: 5.1 V	5.015639564 V	Pass	Eep 14 Mar 2018
8.8. Test RMT3.3	LSL: 3.2 V USL: 3.4 V	3.286850919 V	Pass	Eep 14 Mar 2018
8.9. Test VCC3.3	LSL: 3.2 V USL: 3.4 V	3.374480156 V	Pass	Eep 14 Mar 2018
9. Test Over-Voltage Clamp	PASS	PASS	Pass	Eep 14 Mar 2018
9.1. Test Input Clamping Voltage	LSL: -1.83 V USL: -1.13 V	-1.5 V	Pass	Eep 14 Mar 2018
9.2. Test V_Sat Pulse Width	LSL: 6.2 ns USL: 56.2 ns	40.49075 ns	Pass	Eep 14 Mar 2018
9.3. Test P_PDA Peak Voltage	LSL: 4.096 V USL: 4.5 V	4.271065 V	Pass	Eep 14 Mar 2018
10. Test Charge Amp Speed	PASS	PASS	Pass	Eep 14 Mar 2018
10.1. Signal Rise Time	LSL: 30 ns USL: 150 ns	96.14155 ns	Pass	Eep 14 Mar 2018

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11. Test Linearity	PASS	PASS	Pass	Eep 14 Mar 2018
11.1. Linearity %FS	LSL: -0.05 %FS USL: 0.05 %FS	-0.003663775 %FS	Pass	Eep 14 Mar 2018
11.2. Slope	LSL: -54000 USL: -49000	-51487.615952381	Pass	Eep 14 Mar 2018
12. Test Noise	PASS	PASS	Pass	Eep 14 Mar 2018
12.1. Fixed Noise	LSL: 2 USL: 7	3.605516758	Pass	Eep 14 Mar 2018
12.2. Charge Injection	LSL: 12700 USL: 23100	18284.394871795	Pass	Eep 14 Mar 2018
12.3. Dark Current	LSL: -500 USL: 500	-3.10974359	Pass	Eep 14 Mar 2018
13. Write Flash Memory	PASS	PASS	Pass	Eep 14 Mar 2018
14. Test NVM	PASS	PASS	Pass	Eep 14 Mar 2018

Comments:

N/A Eep 14 Mar 2018

Overall Test Conclusion:

☒ Pass☐ Fail

Waters Corporation - Test Record

Part Number: <u>210001203 Rev A</u>	Product:
Operator: <u>administrator</u>	Start Time: <u>03/14/2018, 11:27:34</u>
Serial Number: <u>261217023M</u>	End Time: <u>03/14/2018, 11:30:21</u>
Test System: <u>TE82988-1</u>	

Name	LSL	Measurement	USL	Unit	Outcome
Test Fixture ID	NaN	4			PASS
Fixture Down Detect					PASS
Test UUT Power					PASS
Measure PS1 (+5V) Voltage	4.8	5	5.2	V	PASS
Measure PS1 (+5V) Current	0.8	0.944	1.2	A	PASS
Measure PS3 (-15V) Voltage	14.7	15.005	15.3	V	PASS
Measure PS3 (-15V) Current	0	0.05	0.1	A	PASS
Measure PS4 (+15V) Voltage	14.7	15.002	15.3	V	PASS
Measure PS4 (+15V) Current	0	0.064	0.1	A	PASS
Report Text		Unprogrammed			PASS
Write Flash Memory					PASS
Disable UUT Power					DONE
Test UUT Power					PASS
Measure PS1 (+5V) Voltage	4.8	5	5.2	V	PASS
Measure PS1 (+5V) Current	0.8	0.918	1.2	A	PASS
Measure PS3 (-15V) Voltage	14.7	15.005	15.3	V	PASS
Measure PS3 (-15V) Current	0	0.05	0.1	A	PASS
Measure PS4 (+15V) Voltage	14.7	15.002	15.3	V	PASS
Measure PS4 (+15V) Current	0	0.065	0.1	A	PASS
Initialize					PASS
Test Onboard Power Supplies					PASS
Test 14A	13.8	13.932871577	14.2	V	PASS
Test N14A	-14.2	-13.978155865	-13.8	V	PASS
Test 5A	4.8	5.015622946	5.1	V	PASS
Test N5A	-5.1	-5.033734571	-4.8	V	PASS
Test PDA_VB	1.998	1.999611215	2.002	V	PASS
Test VREF_2p5	2.4	2.499649048	2.6	V	PASS
Test PDA_5A	4.8	5.015639564	5.1	V	PASS
Test RMT3.3	3.2	3.286850919	3.4	V	PASS
Test VCC3.3	3.2	3.374480156	3.4	V	PASS
Set Offset Register					DONE
Test Over-Voltage Clamp					PASS
Test Input Clamping Voltage	-1.83	-1.5	-1.13	V	PASS
Test V_Sat Pulse Width	6.2	40.49075	56.2	ns	PASS
Test P_PDA Peak Voltage	4.096	4.271065	4.5	V	PASS
Test Charge Amp Speed					PASS
Signal Rise Time	30	96.14155	150	ns	PASS
Test Linearity					PASS
Linearity %FS	-0.05	-0.003663775	0.05	% FS	PASS
Slope	-54000	-51487.615952381	-49000		PASS
Test Noise					PASS
Vacuum Off					DONE
Fixed Noise	2	3.605516758	7		PASS
Charge Injection	12700	18284.394871795	23100		PASS
Dark Current	-500	-3.10974359	500		PASS
Write Flash Memory					PASS
Test NVM					PASS

210001203 Rev A Overall Result - PASS

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Iteration No.: 01
Attachment: 7.3 Page: 1 of 1

Signed: 

Date: 14 March 2018

Signature indicated record was printed from Sigma Quest Database Sep 14 Mar 2018

END OF DATA

Report No: TE0084037-EDV

Iteration No: 01

SAP No: TE0084037QA

Test Name: Fault Insertion Test

Test Script No.: EDV-04

Equipment Number: TE0084037

Equipment Name: Charge Amp PCB Assembly Test Fixture

Software Version: A

Part Number: 210001203

Serial Number: 261217023M

Purpose:

To verify that the equipment will fail a UUT that does not meet the critical to quality specifications under test.

Test execution:

Perform each of the fault insertion tests below. Record the actual result of the test, whether a fault was screened, and initial/date. After each Fault Insertion Method, reverse or remove the physical means of the failure before continuing with the next test.

Objective evidence:

Completed Test Script Data Sheet

Screenshot of equipment software UI showing failure

Requirement	Fault Insertion Method	Expected Result	Actual Results	Fault Screened?	Initial & Date
1. Test UUT Power		FAIL	Failed	Yes	ELP 14 Mar 2018
1.1. Measure PS1 (+5) Voltage	Connect a 2Ω resistor across the VCC and GND test points before starting test.	Fail	Failed 3.194 V	Yes	ELP 14 Mar 2018
1.2. Measure PS1 (+5) Current	Connect a 16Ω resistor across the VCC and GND test points before starting test.	Fail	Failed 1.221 A	Yes	ELP 14 Mar 2018
1.3. Measure PS3 (-15) Voltage	Connect a 25Ω resistor across the N15V and AGND test points before starting test.	Fail	Failed 0.029 V	Yes	ELP 14 Mar 2018
1.4. Measure PS3 (-15) Current	Connect a 200Ω resistor across the N15V and AGND test points before starting test.	Fail	Failed 0.126 A	Yes	ELP 14 Mar 2018
1.5. Measure PS4 (+15) Voltage	Connect a 25Ω resistor across the P15V and AGND test points before starting test.	Fail	Failed 3.534 V	Yes	ELP 14 Mar 2018
1.6. Measure PS4 (+15) Current	Connect a 200Ω resistor across the P15V and AGND test points before starting test.	Fail	Failed 0.140 A	Yes	ELP 14 Mar 2018
2. Test Onboard Power Supplies		FAIL	Failed	Yes	ELP 14 Mar 2018
2.1. Test 14A	Remove the 14A probe before starting test.	Fail	Failed -0.00196158 V	Yes	ELP 14 Mar 2018
2.2. Test N14A	Remove the N14A probe before starting test.	Fail	Failed -0.00157671 V	Yes	ELP 14 Mar 2018
2.3. Test 5A	Remove the 5A probe before starting test.	Fail	Failed -0.001895212 V	Yes	ELP 14 Mar 2018

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2.4. Test N5A	Remove the N5A probe before starting test.	Fail	Failed -0.001507848 V	yes	EEP 14 Mar 2018
2.5. Test PDA_VB	Remove pin 8 in the PDA socket before starting test.	Fail	Failed -0.002125245 V	yes	EEP 14 Mar 2018
2.6. Test VREF_2p5	Remove the VREF_2p5 probe before starting test.	Fail	Failed -0.002032577 V	yes	EEP 14 Mar 2018
2.7. Test PDA_5A	Remove pin 4 in the PDA socket before starting test.	Fail	Failed -0.001823919 V	yes	EEP 14 Mar 2018
2.8. Test RMT3.3	Remove the RMT3.3 probe before starting test.	Fail	Failed -0.001736311 V	yes	EEP 14 Mar 2018
2.9. Test VCC3.3	Remove the VCC3.3 probe before starting test.	Fail	Failed -0.001645713 V	yes	EEP 14 Mar 2018
3. Test Over-Voltage Clamp		FAIL	Failed	yes	EEP 14 Mar 2018
3.1. Set Input Voltage	Disconnect the scope CH1 cable before starting test.	Fail	Failed	yes	EEP 14 Mar 2018
3.2. Test Clamp Pulse Width	Insert a breakpoint at the "Test V_Sat Pulse Width" step in the "Clamping" test sequence. When the test reaches the breakpoint disconnect the scope CH1 cable, push the "Force Trigger" button on the front panel of the scope, then continue.	Fail	Failed 4.3422 ns	yes	EEP 14 Mar 2018
3.3. Test P_PDA Peak Voltage	Disconnect the scope CH2 cable before starting test.	Fail	Failed 0.1072107 V	yes	EEP 14 Mar 2018
4. Test Charge Amp Speed		FAIL	Failed	yes	EEP 14 Mar 2018
4.1. Signal Rise Time	Insert a breakpoint at the "Charge Amp Speed" step in the "Charge" test sequence. When the test reaches the breakpoint disconnect the scope CH2 cable, push the "Force Trigger" button on the front panel of the scope, then continue.	Fail	Failed 4976.9 ns	yes	EEP 14 Mar 2018
5. Test Linearity		FAIL	Failed	yes	EEP 14 Mar 2018
5.1. Slope	Change the "Test Over-Voltage Clamp" and "Test Charge Amp Speed" run modes to "Skip" in the main sequence and remove pin 9 in the PDA socket before starting test.	Fail	Failed -0.062738095	yes	EEP 14 Mar 2018

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6. Test Noise		FAIL	Failed	Yes	Eep 14 Mar 2018
6.1. Fixed Noise	Change the "Vacuum Off" run mode to "Skip" in the "Test Noise" sequence before starting the test.	Fail	Failed 9.956055699	Yes	Eep 14 Mar 2018
7. Test NVM		FAIL	Failed	Yes	Eep 14 Mar 2018
7.1. Test NVM	Insert breakpoint at the "Test NVM" step in the main sequence. When the test reaches the breakpoint disconnect the ribbon cable and continue.	Fail	Failed	Yes	Eep 14 Mar 2018

Comments:

The test step name in §4.1 should be "Cfg TDS CH2 Speed" instead of "Charge Amp Speed" and the test sequence name should be "Charge Amp Speed" instead of "Charge." This is a protocol error.

The test sequence name in §6.1 should be "Fixed Noise" instead of "Test Noise." This is a protocol error.

Eep
14 Mar 2018

Overall Test Conclusion:

☒ Pass☐ Fail