

1.0 Background

The Charge Amp PCB Assembly Test Fixture (TE0084037) is located in the Test Engineering laboratory in Milford, MA. The fixture facilitates the functional test for Charge Amp PCBs of the following part numbers: 210001164 and 210001203. During the test, the UUT is connected and the test program on the GTS is launched. The automated test begins once the UUT serial number has been entered, and the electrical performance of the board is verified. Tests include UUT and onboard power, initialization, NVM, voltage clamp, charge amp speed, linearity, and noise. Upon completion, a Final Test Record is automatically generated and saved to the SigmaSure Database. The operator can elect to print a hard copy of the report as well.

The Production Support Checks listed in the following Traceability Matrices are performed in addition to the required testing in order to verify attributes not defined as critical. These PSC tests ensure the personality board is prepared to engage in functional testing of the UUT.

Note that the Output Specification Documents used as references include specifications that are not applicable to this test. The PCB Manufacturing Test Specifications (Section 5.2 in both Output Specification Documents) are the only specifications relevant to the automated board test administered by the Charge Amp PCB Assembly Test Fixture (TE0084037).

2.0 Definitions and Abbreviations

Term	Definition / Abbreviation
2p5	2.5 V
A	Amps
AGND	Analog Ground
CA	Charge Amp
CHx	Channel (x denotes which channel)
EDV(R)	Equipment Design Verification (Report)
FS	Full Scale
GND	Ground
GTS	Global Test System (multifunctional generic PCB functional test system)
N	Negative
ns	Nanoseconds
NVM	Non-Volatile Memory
P	Positive
PCB	Printed Circuit Board
PDA	Photodiode Array
PIX	Pixel
P/N	Part Number
PSC	Production Support Check
PSx	Power Supply (x denotes which power supply)
RMT	Remote

Traceability Matrix for (TE0084037)

Report No: TE0084037-Memo

Iteration No: 01

SAP No: TE0084037EQ

SAP	Enterprise Resource Planning (ERP) software
Sat	Saturated
SN	Serial Number
TSP	Test Specification and Procedure
UI	User Interface
UUT	Unit Under Test
V	Volts
VB	Voltage Bias
VCC	Integrated Circuit Power Supply Voltage
VREF	Reference Voltage
x	Test Variable
Ω	Ohm

3.0 References / Related Documents

Doc No / SAP Directory	Document Title
730001835	Process Validation Procedure for Milford Site
730002845	Validation Report Template
730001833	Test Engineering Management Policy
735002109, Ver. 00	Waters GTS Operation TSP
735004006, Ver. 00	Waters GTS Preventative Maintenance and Calibration Procedure
TE0084037EQ	Equipment Design Documentation
721014067	210001164 Output Specification
721015389	210001203 Output Specification

 THE SCIENCE OF WHAT'S POSSIBLE.™	Traceability Matrix for (TE0084037)		
Report No: TE0084037-Memo	Iteration No: 01	SAP No: TE0084037EQ	

4.0 Traceability Matrices

Equipment Number: TE0084037		Equipment Name: Charge Amp PCB Assembly Test Fixture	
Software Version: A		Part Number: 210001164	
Description of Test	Acceptance Criteria	Reference	
Test Fixture ID			
Test Fixture ID	4	PSC: Pre-test Condition	
Fixture Down Detect			
Fixture Down Detect	PASS	PSC: Pre-test Condition to verify UUT functionality	
Test UUT Power			
Measure PS1 (+5) Voltage	LSL: 4.8 V USL: 5.2 V	PSC: Pre-test Condition to verify UUT functionality. Range is determined by standard industry practice.	
Measure PS1 (+5) Current	LSL: 0.8 A USL: 1.2 A		
Measure PS3 (-15) Voltage	LSL: 14.7 V USL: 15.3 V		
Measure PS3 (-15) Current	LSL: 0 A USL: 0.1 A		
Measure PS4 (+15) Voltage	LSL: 14.7 V USL: 15.3 V		
Measure PS4 (+15) Current	LSL: 0 A USL: 0.1 A		
Initialize			
Initialize	PASS	PSC: Pre-test Condition to verify UUT functionality.	
Test Onboard Power Supplies			
Test 14A	LSL: 13.8 V USL: 14.2 V	PSC: Pre-test Condition to verify board functionality. Range is determined by standard industry practice.	
Test N14A	LSL: -14.2 V USL: -13.8 V		
Test 5A	LSL: 4.8 V USL: 5.1 V		
Test N5A	LSL: -5.1 V USL: -4.8 V		
Test PDA_VB	LSL: 1.998 V USL: 2.002 V		
Test VREF_2p5	LSL: 2.4 V USL: 2.6 V		
Test PDA_5A	LSL: 4.8 V USL: 5.1 V		

Traceability Matrix for (TE0084037)

Report No: TE0084037-Memo

Iteration No: 01

SAP No: TE0084037EQ

Test RMT3.3	LSL: 3.2 V USL: 3.4 V	
Test VCC3.3	LSL: 3.2 V USL: 3.4 V	
Test NVM		
Test NVM	PASS	PSC: Functional Test
Set Offset Register		
Set Offset Register	DONE	PSC: Functional Test
Test Over Voltage Clamp		
Test Input Clamping Voltage	LSL: -1 V USL: -0.3 V	PSC: Fixture Check
Test V_Sat Pulse Width	LSL: 25 ns USL: 75 ns	PSC: Extra Test
Test P_PDA Peak Voltage	LSL: 4.096 V USL: 4.5 V	Specified in 721014067, Ver. 01, Sec. 5.2.4.1
Test Charge Amp Speed		
Signal Rise Time	LSL: 30 ns USL: 150 ns	PSC: Extra Test
Test Linearity		
Linearity %FS	LSL: -0.05 %FS USL: 0.05 %FS	Specified in 721014067, Ver. 01, Sec. 5.2.2
Slope	LSL: -78500 USL: -75000	PSC: Fixture Check
Test Noise		
Vacuum Off	DONE	PSC: Pre-test Condition
Fixed Noise	LSL: 2 USL: 7	Specified in 721014067, Ver. 01, Sec. 5.2.1
Charge Injection	LSL: 8000 USL: 18400	Specified in 721014067, Ver. 01, Sec. 5.2.4.2
Dark Current	LSL: -500 USL: 500	Specified in 721014067, Ver. 01, Sec. 5.2.5

 THE SCIENCE OF WHAT'S POSSIBLE.™	Traceability Matrix for (TE0084037)		
Report No: TE0084037-Memo	Iteration No: 01	SAP No: TE0084037EQ	

Equipment Number: TE0084037		Equipment Name: Charge Amp PCB Assembly Test Fixture	
Software Version: A		Part Number: 210001203	
Description of Test	Acceptance Criteria	Reference	
Test Fixture ID			
Test Fixture ID	4	PSC: Pre-test Condition	
Fixture Down Detect			
Fixture Down Detect	PASS	PSC: Pre-test Condition to verify UUT functionality	
Test UUT Power			
Measure PS1 (+5) Voltage	LSL: 4.8 V USL: 5.2 V	PSC: Pre-test Condition to verify UUT functionality. Range is determined by standard industry practice.	
Measure PS1 (+5) Current	LSL: 0.8 A USL: 1.2 A		
Measure PS3 (-15) Voltage	LSL: 14.7 V USL: 15.3 V		
Measure PS3 (-15) Current	LSL: 0 A USL: 0.1 A		
Measure PS4 (+15) Voltage	LSL: 14.7 V USL: 15.3 V		
Measure PS4 (+15) Current	LSL: 0 A USL: 0.1 A		
Report Text			
Report Text	Unprogrammed	PSC: Pre-test Condition	
Write Flash Memory			
Write Flash Memory	PASS	PSC: Pre-test Condition	
Disable UUT Power			
Disable UUT Power	DONE	PSC: Pre-test Condition	
Test UUT Power			
Measure PS1 (+5) Voltage	LSL: 4.8 V USL: 5.2 V	PSC: Pre-test Condition to verify UUT functionality. Range is determined by standard industry practice.	
Measure PS1 (+5) Current	LSL: 0.8 A USL: 1.2 A		
Measure PS3 (-15) Voltage	LSL: 14.7 V USL: 15.3 V		
Measure PS3 (-15) Current	LSL: 0 A USL: 0.1 A		
Measure PS4 (+15) Voltage	LSL: 14.7 V USL: 15.3 V		
Measure PS4 (+15) Current	LSL: 0 A USL: 0.1 A		

Traceability Matrix for (TE0084037)

Report No: TE0084037-Memo

Iteration No: 01

SAP No: TE0084037EQ

Initialize		
Initialize	PASS	PSC: Pre-test Condition to verify UUT functionality.
Test Onboard Power Supplies		
Test 14A	LSL: 13.8 V USL: 14.2 V	PSC: Pre-test Condition to verify board functionality. Range is determined by standard industry practice.
Test N14A	LSL: -14.2 V USL: -13.8 V	
Test 5A	LSL: 4.8 V USL: 5.1 V	
Test N5A	LSL: -5.1 V USL: -4.8 V	
Test PDA_VB	LSL: 1.998 V USL: 2.002 V	
Test VREF_2p5	LSL: 2.4 V USL: 2.6 V	
Test PDA_5A	LSL: 4.8 V USL: 5.1 V	
Test RMT3.3	LSL: 3.2 V USL: 3.4 V	
Test VCC3.3	LSL: 3.2 V USL: 3.4 V	
Set Offset Register		
Set Offset Register	DONE	PSC: Functional Test
Test Over Voltage Clamp		
Test Input Clamping Voltage	LSL: -1.83 V USL: -1.1 V	PSC: Fixture Check
Test V_Sat Pulse Width	LSL: 6.2 ns USL: 56.2 ns	PSC: Extra Test
Test P_PDA Peak Voltage	LSL: 4.096 V USL: 4.5 V	Specified in 721015389, Ver. 00, Sec. 5.2.4.1
Test Charge Amp Speed		
Signal Rise Time	LSL: 30 ns USL: 150 ns	PSC: Extra Test
Test Linearity		
Linearity %FS	LSL: -0.05 %FS USL: 0.05 %FS	Specified in 721015389, Ver. 00, Sec. 5.2.2
Slope	LSL: -53350 USL: -49850	PSC: Fixture Check

 THE SCIENCE OF WHAT'S POSSIBLE.™	Traceability Matrix for (TE0084037)	
Report No: TE0084037-Memo	Iteration No: 01	SAP No: TE0084037EQ

Test Noise		
Vacuum Off	DONE	PSC: Pre-test Condition
Fixed Noise	LSL: 2 USL: 7	Specified in 721015389, Ver. 00, Sec. 5.2.1
Charge Injection	LSL: 12700 USL: 23100	Specified in 721015389, Ver. 00, Sec. 5.2.4.2
Dark Current	LSL: -500 USL: 500	Specified in 721015389, Ver. 00, Sec. 5.2.5
Write Flash Memory		
Write Flash Memory	PASS	PSC: Pre-test condition
Test NVM		
Test NVM	PASS	PSC: Functional Test