

WATERS CORPORATION

PERFORMANCE SPECIFICATION

TYPE OF SPECIFICATION (check one):

☐

SYSTEM

☒ SUB ASSEMBLY

PRODUCT: ALLIANCE

DOCUMENT NUMBER:810000384

ASSEMBLY NAME:PCB, ALLIANCE FRONT
PANEL

REVISION: A

PART NUMBER AFFECTED: 210000384

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DATE: July 24, 2009

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REVISION HISTORY:

<u>REV.</u>	<u>DWO/ECO NO.</u>	<u>DATE</u>	<u>ORIGINATOR</u>
A		7/24/09	B. Deguire

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INTRODUCTION

Document Intent

The intent of this document is to provide a description and performance specifications for the Alliance Front Panel PCB design. Specifications for software programmers and the system are given. Information as to how this design is utilized and controlled by software is not included.

The original design, created by Roger Gilman, was 270022 which is available for reference in SAP. The corresponding PRF is 270620. The new part number of 210000384 was assigned due to changes that are not backwards compatible and being converted to RoHS compliance. The functional difference is the backlight change from CCFL to LED.

Related Documents

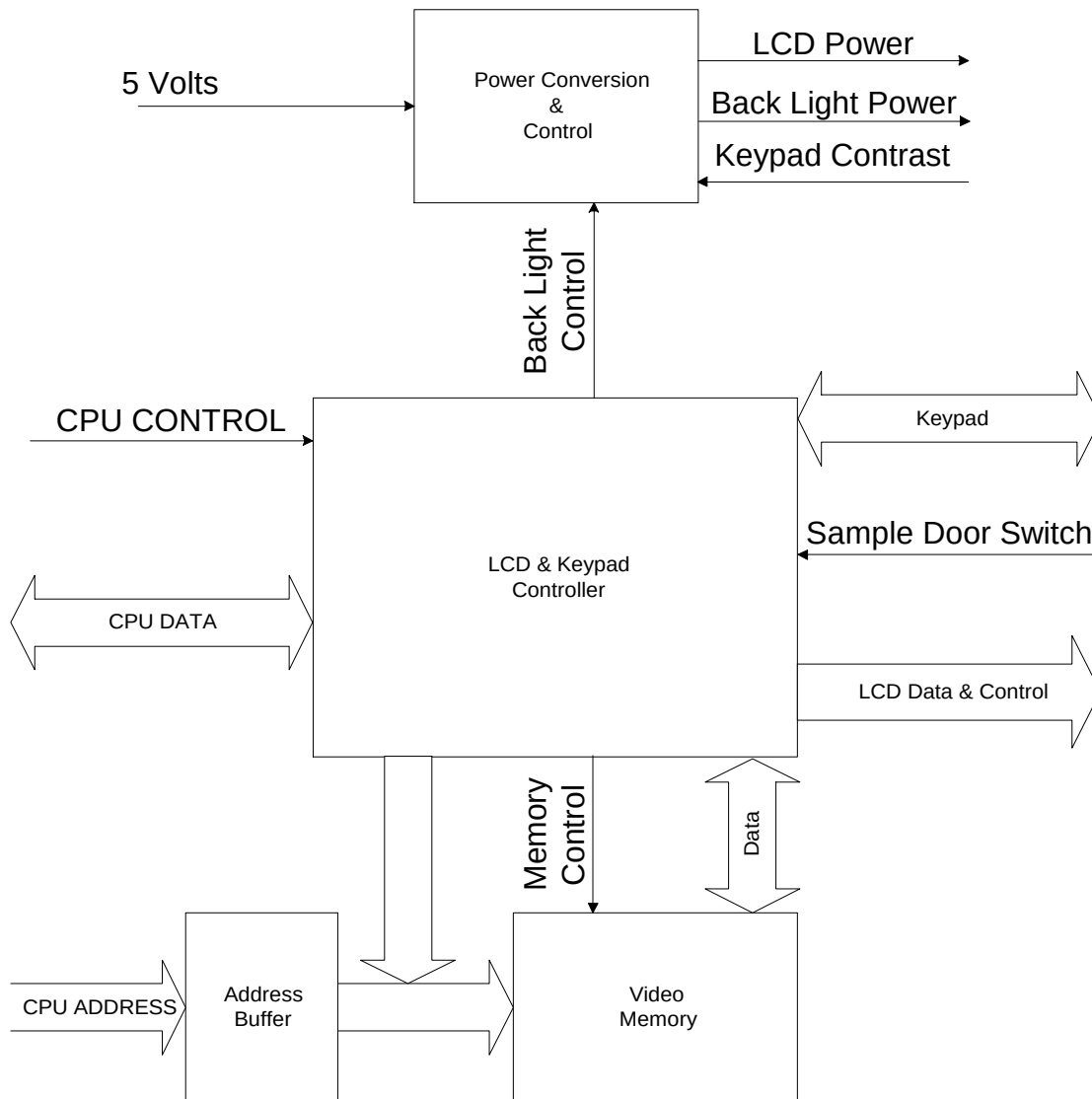
710000384	Schematic, PCB, Alliance Front Panel
510000384	PCB, Alliance Front Panel
610000384	A/W, PCB, Alliance Front Panel
210000384	Assy, PCB, Alliance Front Panel
270133	Keypad, Fluidics Module

ASSEMBLY DESCRIPTION

Introduction

The front panel PCB design includes all circuitry to interface and drive the LCD panel with back lighting and contrast control, the keypad matrix, and the sample compartment door switch. The interface to the CPU is an eight bit buffered extension of the microcontroller bus. The board is powered with 5 volts by a cable that comes directly from the power supply. One of the intents of this design is to insulate the CPU from changes in keypad or display obsolescence. This has been done by placing only those functions which are directly related to the keypad and LCD on this board. Also, the CPU interface is designed so that other microcontroller designs may be easily made to interface with this board without any modifications to this design.

Block Diagram



Memory Map

Address Range	Device	Size	R/W
0000 to 7FFF	VIDEO MEMORY	Byte	Both
8000	FRONT PANEL INT STATUS	Byte	Read
8001	KEYPAD DATA REGISTER	Byte	Read
8001	BACK LIGHT CONTROL	Byte	Write
E000	LCD PAGE REGISTER	Word	Write

Hardware Specific Register Definitions

Address: 0x8000 Read Only		
Name: Front Panel Interrupt Status Register		
Initial Value: XX		
<u>Bit</u>	<u>Name</u>	<u>Description</u>
7	NU	Not Used, read as 0
6	NU	Not Used, read as 0
5	NU	Not Used, read as 0
4	NU	Not Used, read as 0
3	NU	Not Used, read as 0
2	DRCHGE	Door Position Changed Interrupt
1	KEYUP	Key Up Interrupt
0	KEYDWN	Key Down Interrupt

Address: 0x8001 Read Only		
Name: Keypad Data Register		
Initial Value: XX		
<u>Bit</u>	<u>Name</u>	<u>Description</u>
7	DROPEN	Door Open Status, 1 active
6	DRCLOSE	Door Closed Status, 1 active
5	NU	Not Used, read as 0
4	KEY4	Keypad Data
3	KEY3	
2	KEY2	
1	KEY1	
0	KEY0	

Address: 0x8001 Write Only Name: Back Light Control Register Initial Value: XX		
<u>Bit</u>	<u>Name</u>	<u>Description</u>
7	NU	Not Used
6	NU	Not Used
5	NU	Not Used
4	NU	Not Used
3	NU	Not Used
2	NU	Not Used
1	NU	Not Used
0	BLCNTRL	Back Light Control 0 = Bright, 1 = Dim

Address: 0xE000 Write Only Name: LCD Page Register Initial Value: XXXX		
<u>Bit</u>	<u>Name</u>	<u>Description</u>
15	NU	Not Used
14	BADDR14	LCD Video Base Address Register
13	BADDR13	
12	BADDR12	
11	BADDR11	
10	BADDR10	
9	BADDR9	
8	BADDR8	
7	BADDR7	
6	BADDR6	
5	BADDR5	
4	BADDR4	
3	BADDR3	
2	BADDR2	
1	BADDR1	
0	BADDR0	

Video Memory to LCD Mapping

The LCD panel controlled by this PCB assembly is physically rotated 180 degrees. This was done for mechanical fit reasons. Normally the LCD is scanned left to right, top to bottom. Because the LCD is rotated 180 degrees, the scanning now takes place from right to left, bottom to top and all display images are upside down. To flip the image without impacting software, the bit translation is done in hardware. Two translations take place to flip the image, the first reorders the bits within each byte between the video memory and the display. The second translation inverts the addressing of the bytes from the video memory to the display. The translation is such that bit 7 of the first byte of the selected video memory is mapped to the upper left pixel of the rotated display. Bit 6 of the first byte is mapped to the second pixel and so on, through video memory.

The video memory is bit mapped to the LCD pixels. Each pixel requires one bit of video memory. There are 76800 LCD pixels which require 9600 bytes of memory. The video memory is 32 kilobytes in size. Only 9600 are required to display one screen of the LCD. Up to three full screens may be stored in the video memory. The displayed screen is selected by changing the content of the LCD Base Address Register. The register actually points to the last byte on the screen in video memory.

Keypad Mapping

The keypad is a 32 key matrix organized as 4 columns and 8 rows. The lower two bits of the Keypad Data Register contain the column and the upper three bits contain the row. The pin out of the connector is compatible with the 717 and 600 products. The key to column/row mapping for the Supermodule may be found on the keypad drawing which is referenced at the beginning of this document. The code to row/column and key mapping is shown below:

Code	Row	Column	Key
0x00	1	1	SOFT KEY 3
0x01	1	2	SOFT KEY 2
0x02	1	3	SOFT KEY 1
0x03	1	4	SOFT KEY 4
0x04	2	1	EXIT
0x05	2	2	ENTER
0x06	2	3	MENU/STATUS
0x07	2	4	STOP FLOW
0x08	3	1	0
0x09	3	2	.
0x0A	3	3	CLEAR
0x0B	3	4	SOFT KEY 6
0x0C	4	1	7
0x0D	4	2	8
0x0E	4	3	9
0x0F	4	4	SOFT KEY 5
0x10	5	1	4
0x11	5	2	5
0x12	5	3	6
0x13	5	4	NOT USED
0x14	6	1	1
0x15	6	2	2
0x16	6	3	3
0x17	6	4	NOT USED
0x18	7	1	LEFT ARROW
0x19	7	2	DOWN ARROW
0x1A	7	3	RIGHT ARROW
0x1B	7	4	NOT USED
0x1C	8	1	LEFT HOME ARROW
0x1D	8	2	UP ARROW

0x1E	8	3	RIGHT HOME ARROW
0x1F	8	4	HELP

PCB Pin	Keypad Pin	Column/Row
14	2	Column 1
13	3	Column 2
12	4	Column 3
11	5	Column 4
10	6	Row 1
9	7	Row 2
8	8	Row 3
5	11	Row 4
4	12	Row 5
3	13	Row 6
2	14	Row 7
1	15	Row 8

NOTE: The Keypad pin outs are reversed from the PCB pin outs

Sample Door Switch

The state of the sample compartment door is available to the microcontroller through this board. An interrupt is generated each time the state changes. The state of the door is read along with the keypad data. The switch is open when the door is open.

Back Light And Contrast Control

The LED backlight is connected to the 5 volt supply. A series resistance of 16.5 ohms is used in DIM mode and 1.5 ohms is used for full power. The intent of the 1.5 ohm resistor is to limit the maximum voltage which should extent the life of the LED backlight.

Contrast voltage for the LCD is provided by a LM2611 1.4MHZ Cuk converter which generates -23 volts from the 5 volt power. Contrast adjustment is controlled with the dedicated up and down arrow switches on the front panel keypad, a digital pot connected to these switches and a LM358A opamp. The digital pot changes one bit when pulsed and will move continuously in the direction selected after holding the switched depressed for one second. The opamp, which is power by 5 volts and -23 volts, outputs from -7.5 volts to -22.5 volts for a full contrast change in the LCD.

CPU Interface

The interface between the Front Panel PCB and the host CPU is designed as an extension of the microcontroller address, data and control busses. The address space of the Front Panel board is mapped directly into the address space of the microcontroller on the CPU board. The data bus width is 8 bits and the total address space used is 64 Kbytes. A single chip select along with the read/write signal initiate accesses from the CPU. The Front Panel board responds with an acknowledge signal to terminate access cycles. Access cycles are not fixed in duration because both the CPU and LCD controller are accessing the video memory simultaneously. Priority is given to the LCD controller so that there is no flicker on the LCD. Locally on this board the data and address busses between the LCD controller and the video memory are isolated from the CPU busses. This is done so that both the LCD controller and CPU can access the video memory. This type of interface minimizes design complexity and doesn't sacrifice data bus bandwidth of the CPU. The CPU is notified of events generated on this board by an interrupt. Events that generate an interrupt are; sample door open, sample door close, keypad key depressed and keypad key released. The CPU can poll the appropriate addresses to determine the exact source of the interrupt.

PERFORMANCE SPECIFICATIONS

Keypad

Matrix Size	4 by 8
Scan Rate	140 Hz
Key Debounce Time	7.2 msec

LCD

Scan Rate	74.4 Hz
Video RAM Access Rate	714.3 KHz

Door Open Switch

Switch Type	2 lead SPST magnetic
Switch Debounce Time	13.4 msec

LCD Back Light Control

Voltage	5 Volts
Bright Current	150 mA typical
Dim Current	75 mA typical

LCD Contrast Control

Voltage Range	-7.5 to -22.5 volts
Current	25 mA maximum
Adjustment Resolution	64 steps

CPU Interface

Interface Type	asynchronous microprocessor with DTACK
Connector	40 pin IDC header
Address Range	64 Kbytes
Data Bus Width	8 bits
Maximum Access Time	1 usec

Power

Voltage	5.0 $\pm$ 5%
Current With Display	250 mA maximum

Environmental

Operating	
Temperature Range	0 to 40 °C
Humidity Range	10 to 90% (non-condensing)
Storage	
Temperature Range	-40 to 70 °C
Humidity Range	0 to 100% (non-condensing)