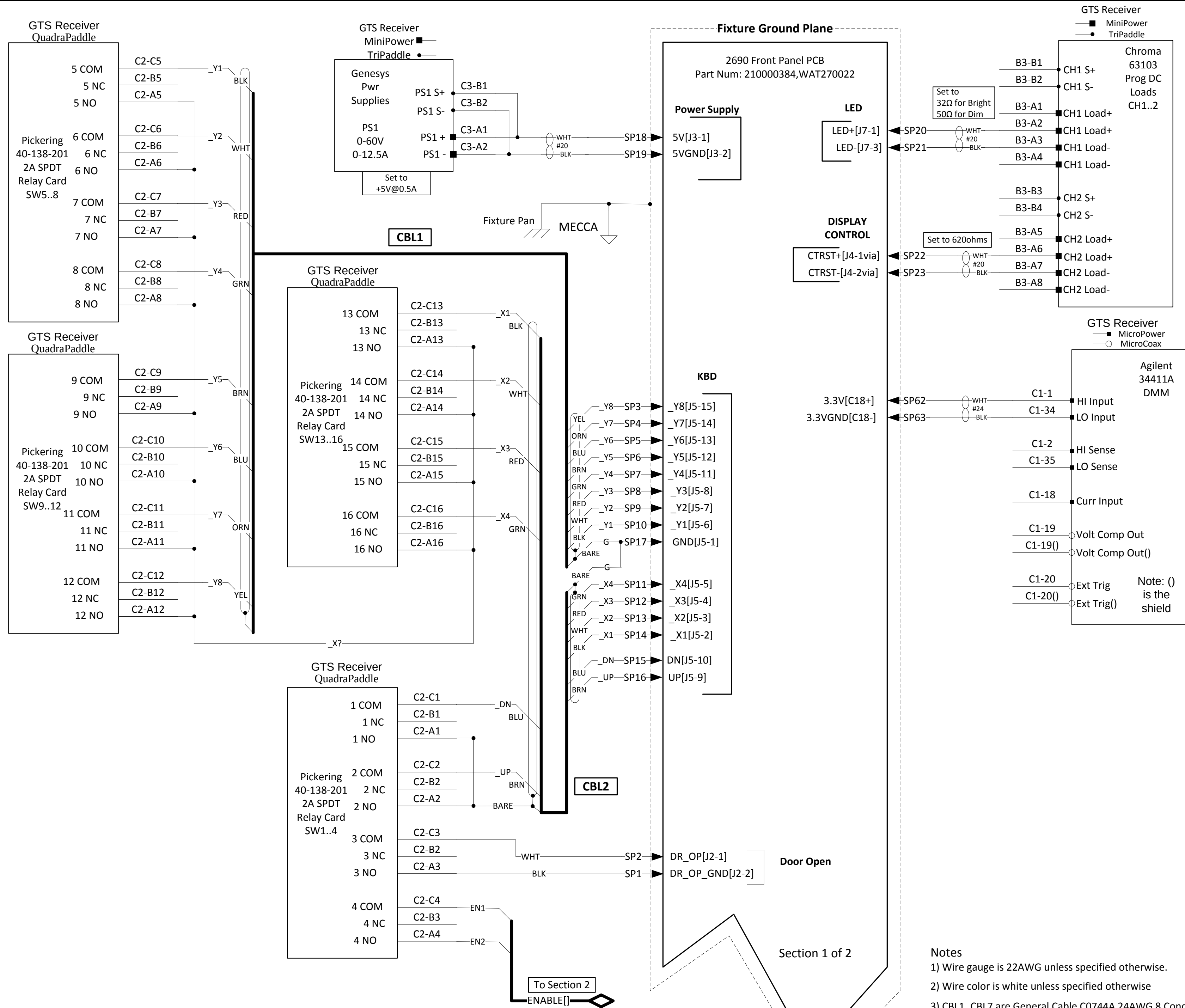
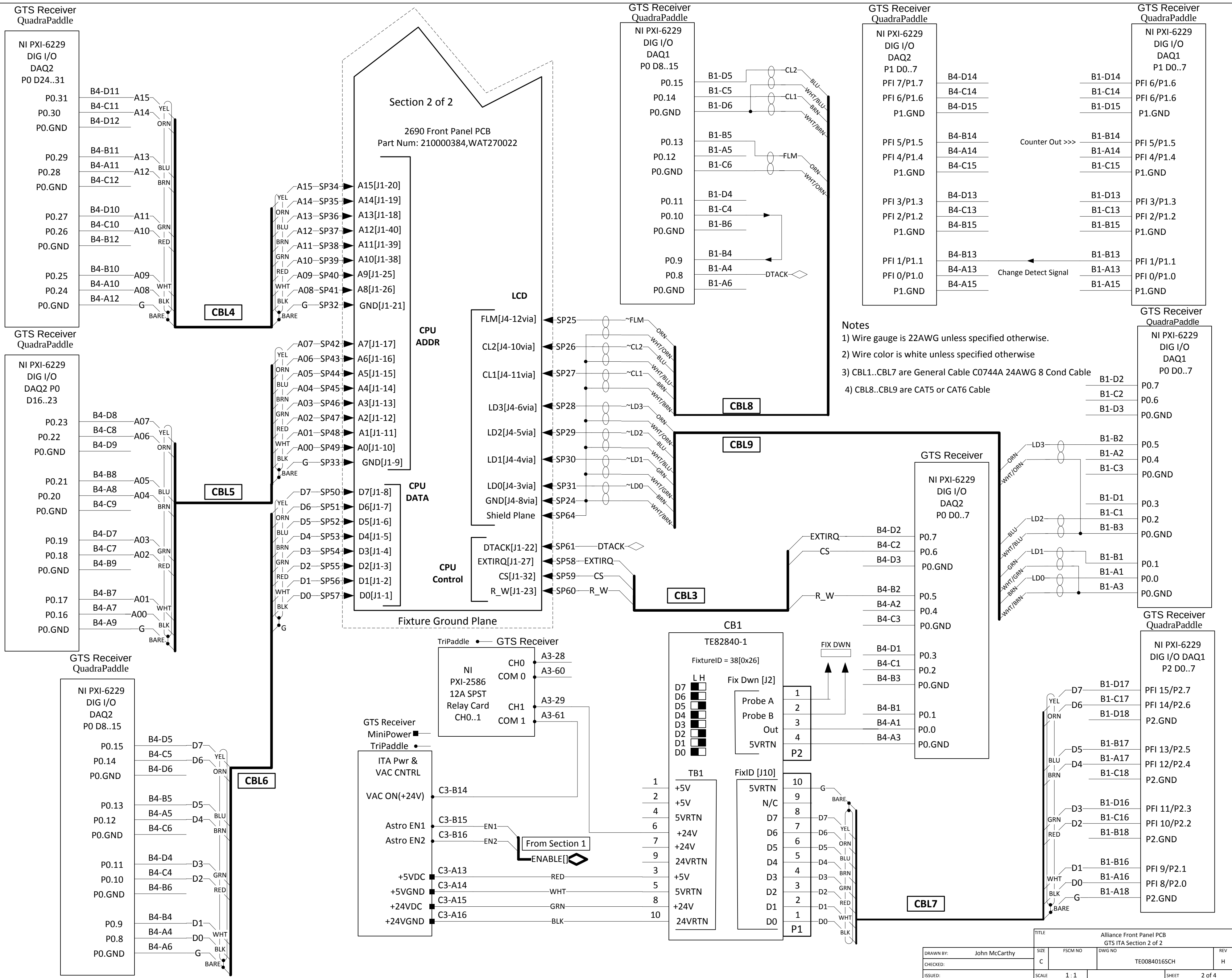


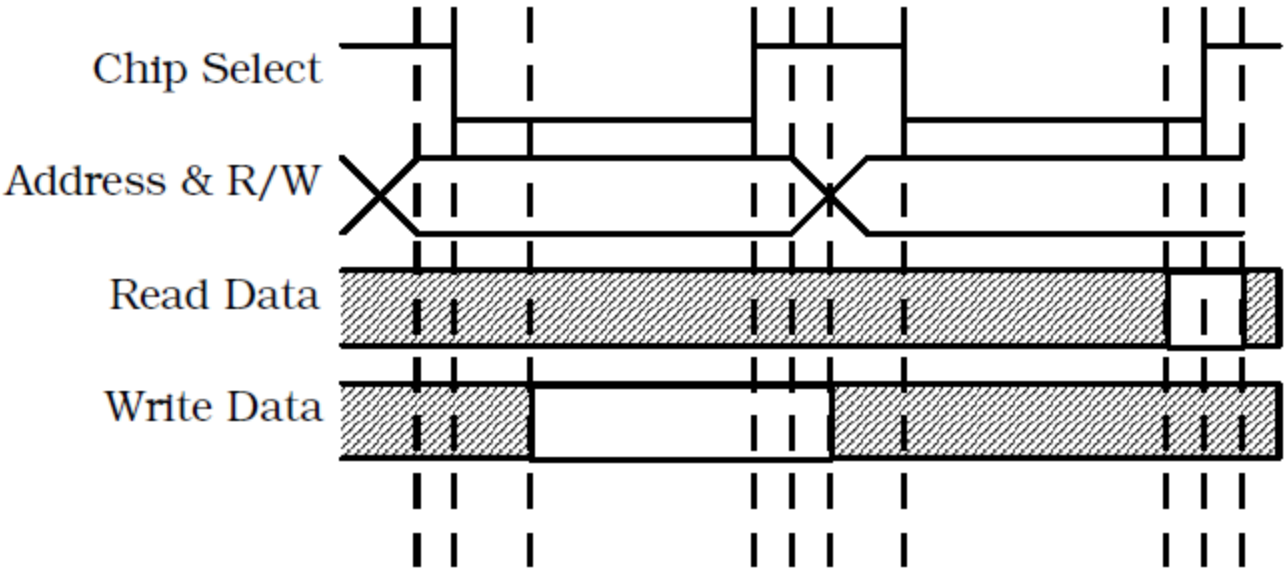
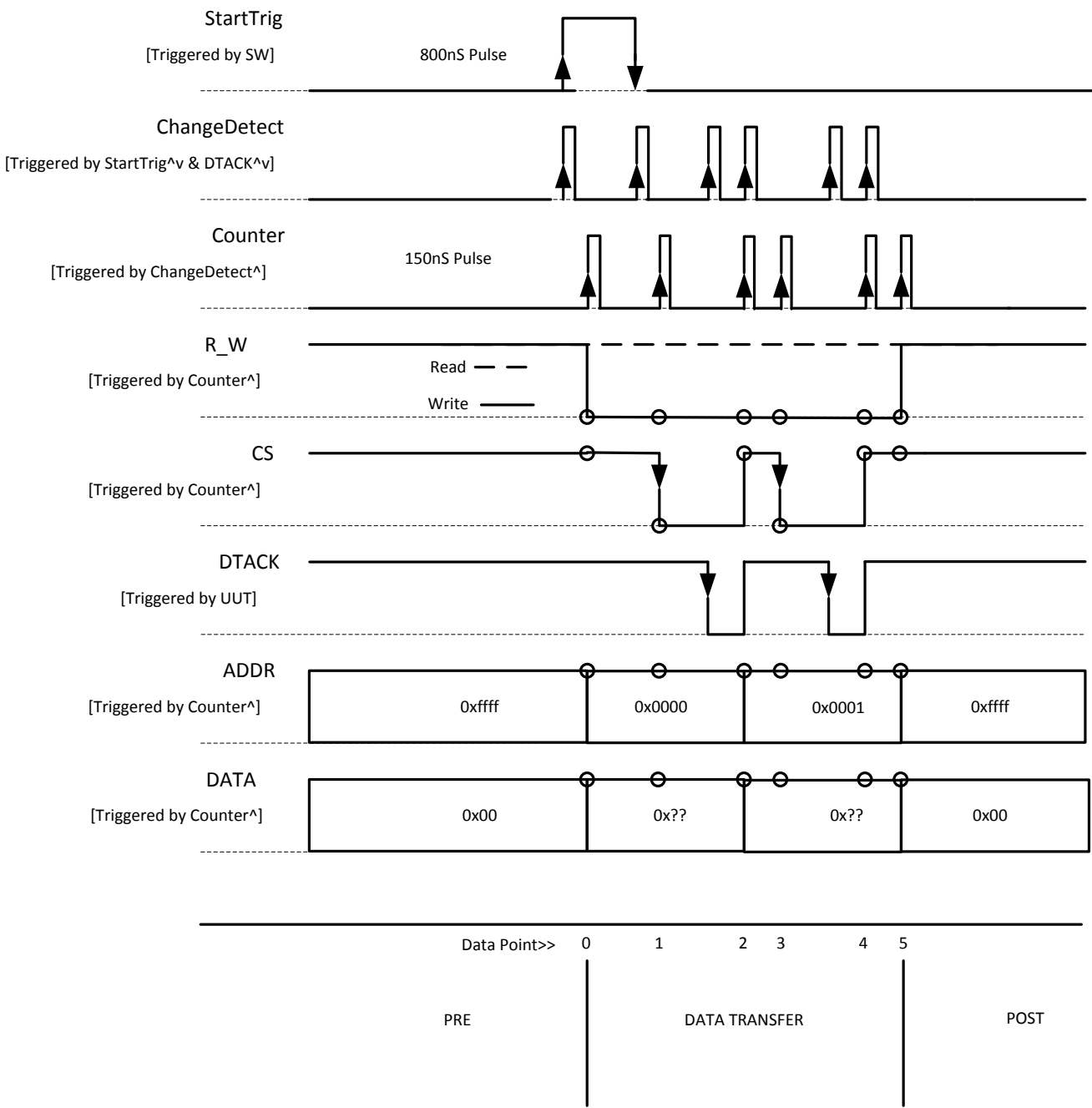


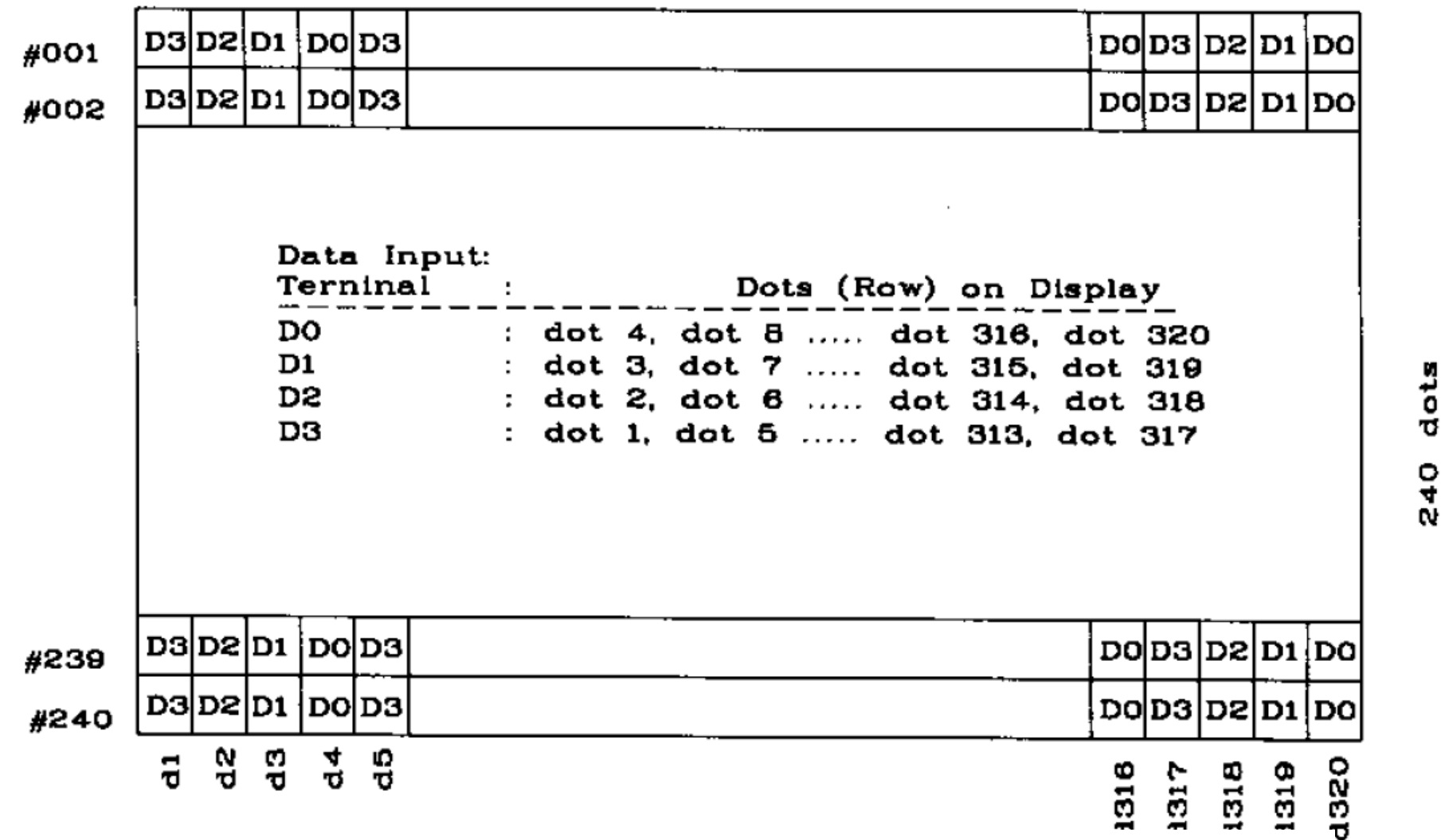


Digital I/O Usage					
DAQ	Port	Line	Type	Timing	Function
1	0	0..7	Input Waveform		Pump Driver Ouputs
		8..12	Input Waveform		SPIDEVSEL & CLK
		13..15	Unused		
		16..23	Unused		
		24..31	Input/Output Waveform		Pump DriverLow Speed I/O
2	1	0..7	Input Waveform	N/A	Motor Encoder
		2	Ouput	N/A	Event Out
	0	0..1	Unused		
		2..7	Output Waveform		Fluidics TPUBUSS
		8..15	Input/Output Waveform		CPU Ext Data
		16..26	Output Waveform		CPU Addr
		27	Output Waveform		FrontPanel CS
		28	Output Waveform		EXTRST
		29	Input		EXTIRQ
		30	Input		EXTDACK
		31	Input		Fixture Down
	1	0..2	Output	N/A	EVENT IN
		3..5	Input	N/A	Buff Selects
		6	Output	N/A	Fluidic CLK
		7	Unused	N/A	
	2	0..7	Input	N/A	Fixture ID Code

PINOUT TABLE															
KEYS	PINS														
	1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5	ROW 6	ROW 7	ROW 8	9	10	ROW 11	ROW 12	ROW 13	ROW 14	ROW 15
S1		•													•
S2			•												•
S3				•											•
S4					•										•
S5		•												•	
S6			•											•	
S7				•										•	
S8		•											•		
S9			•										•		
S10	•									•					
S11		•		•									•		
S12			•									•			
S13				•								•			
S14	•								•						
S15				•								•			
S16		•									•				
S17			•								•				
S18				•							•				
S19		•						•							
S20			•					•							
S21				•				•							
S22			•				•								
S23				•		•									
S24			•			•									
S25		•				•									
S26					•	•									
S27					•					•					
S28					•			•							
S29		•						•							
S30				•			•								
S31					•		•								

NOTE: SWITCH MATRIX IS 4 COLUMNS BY 8 ROWS





PIN NO.	SYMBOL	FUNCTION
1	V _o	OPERATING VOLTAGE FOR LC DRIVING
2	VEE	-23V (POWER SUPPLY FOR LC DRIVING)
3	D0	DATA 0 H-ON (WHITE) L-OFF (BLUE)
4	D1	DATA 1 H-ON (WHITE) L-OFF (BLUE)
5	D2	DATA 2 H-ON (WHITE) L-OFF (BLUE)
6	D3	DATA 3 H-ON (WHITE) L-OFF (BLUE)
7	D-OFF	DISPLAY ENABLE SIGNAL H-ON L-OFF
8	V _{ss}	GND
9	V _{dd}	+5V (POWER SUPPLY FOR LOGIC)
10	CL2	CLOCK SIGNAL FOR SHIFTING THE SERIAL DATA
11	CL1	THE CL1 LATCHES THE SERIAL DATA
12	FLM	THE FLM SIGNAL INDICATES THE BEGINNING OF EACH DISPLAY CYCLE

Cable to connect to J4 Video Connector Molex 210390051

Video Memory to LCD Mapping

The LCD panel controlled by this PCB assembly is physically rotated 180 degrees. This was done for mechanical fit reasons. Normally the LCD is scanned left to right, top to bottom. Because the LCD is rotated 180 degrees, the scanning now takes place from right to left, bottom to top and all display images are upside down. To flip the image without impacting software, the bit translation is done in hardware. Two translations take place to flip the image, the first reorders the bits within each byte between the video memory and the display. The second translation inverts the addressing of the bytes from the video memory to the display. The translation is such that bit 7 of the first byte of the selected video memory is mapped to the upper left pixel of the rotated display. Bit 6 of the first byte is mapped to the second pixel and so on. through video memory.

The video memory is bit mapped to the LCD pixels. Each pixel requires one bit of video memory. There are 76800 LCD pixels which require 9600 bytes of memory. The video memory is 32 kilobytes in size. Only 9600 are required to display one screen of the LCD. Up to three full screens may be stored in the video memory. The displayed screen is selected by changing the content of the LCD Base Address Register. The register actually points to the last byte on the screen in video memory.