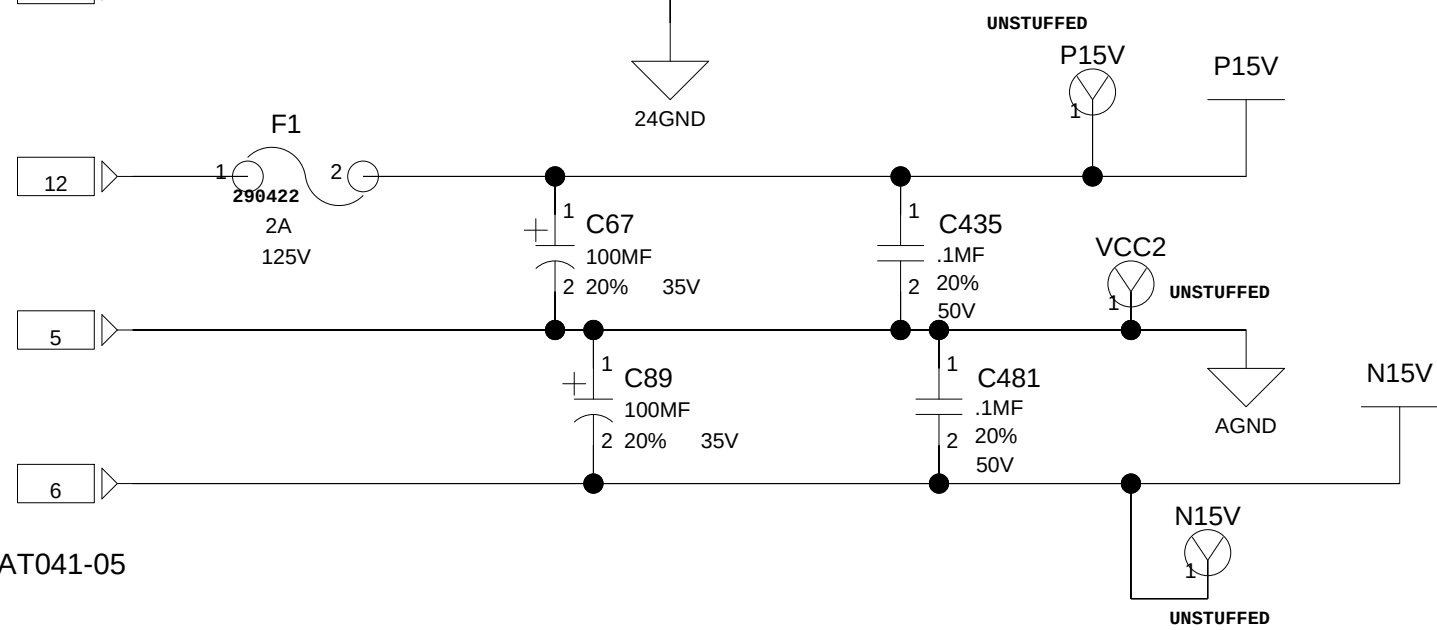
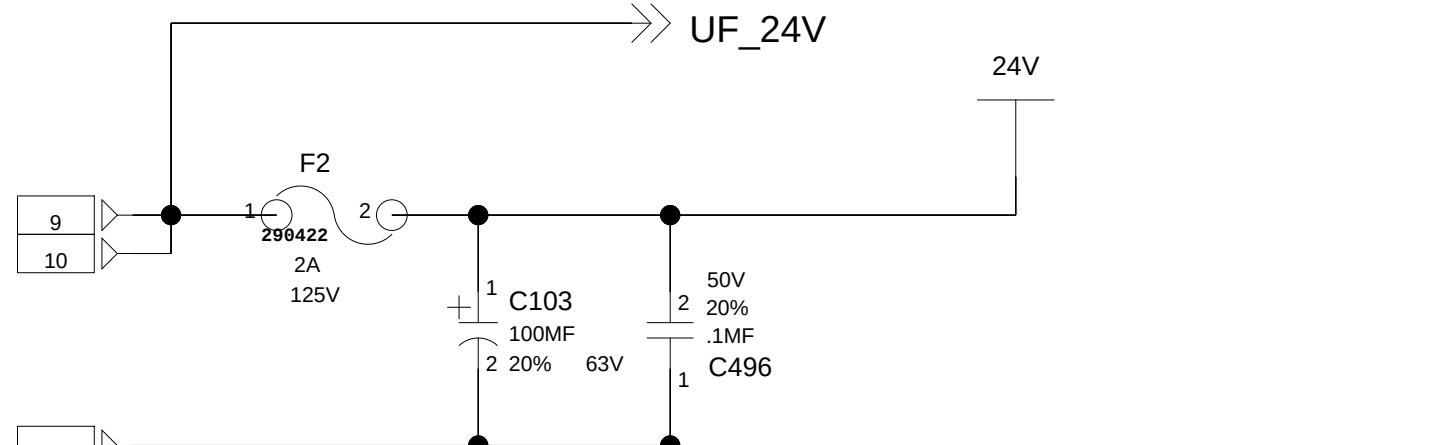
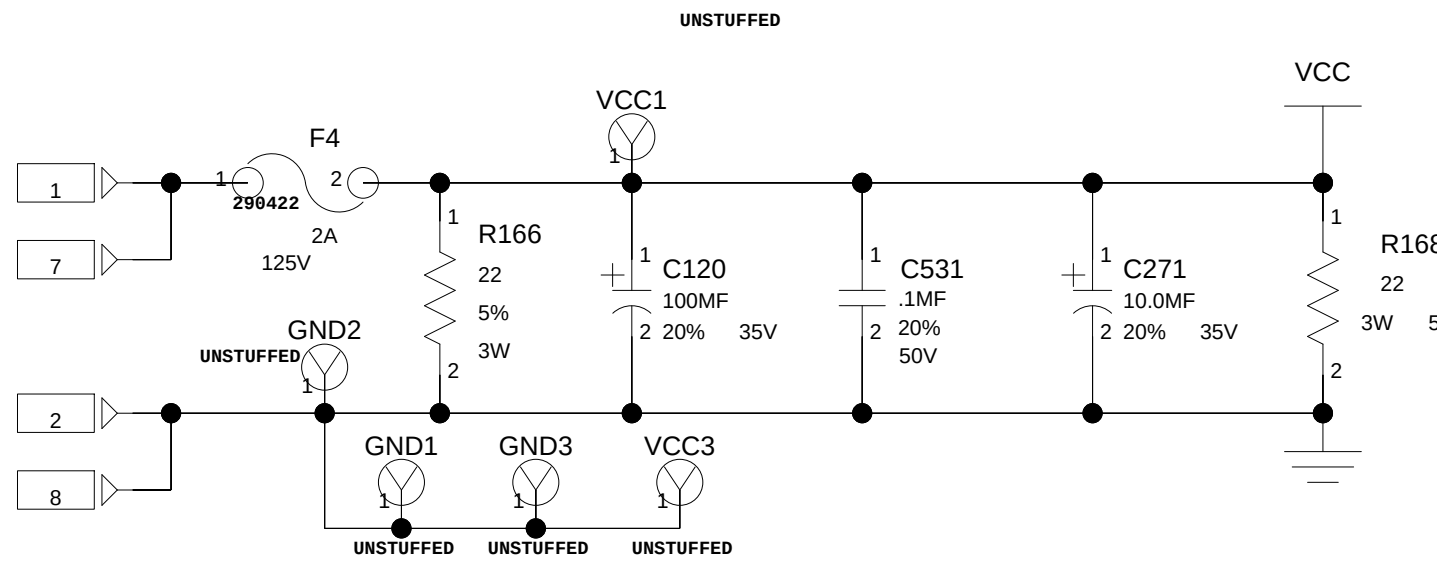
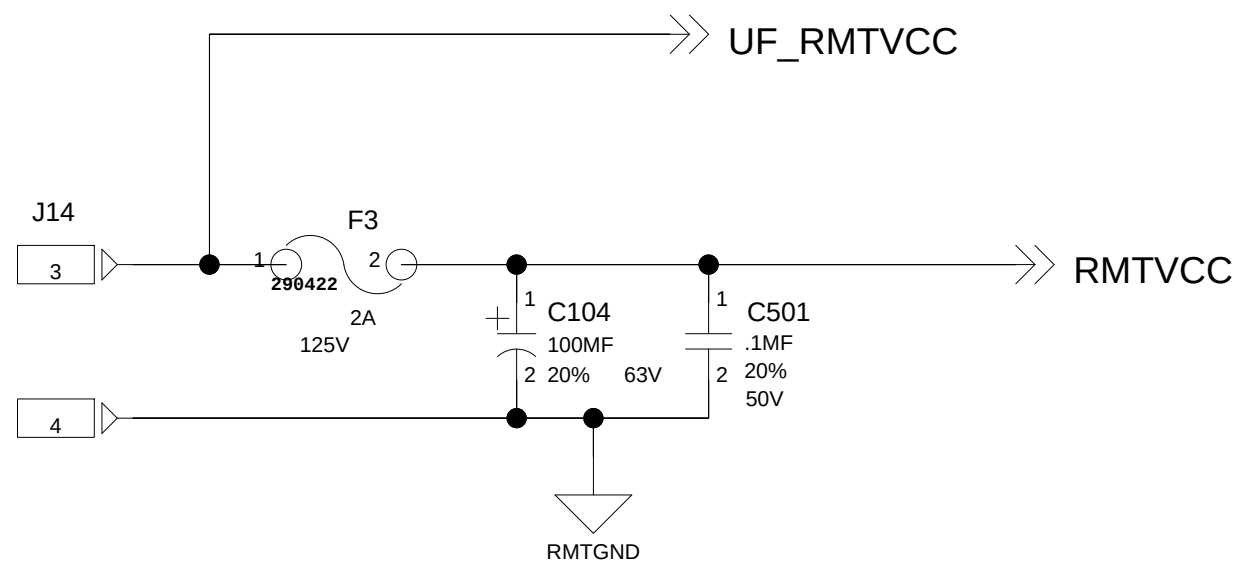
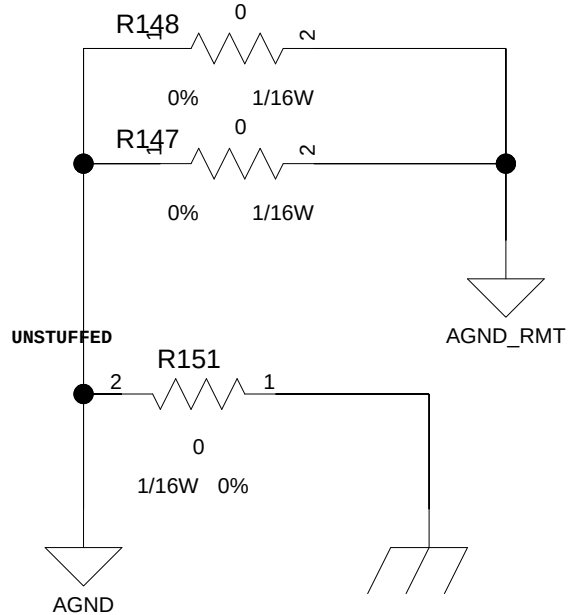
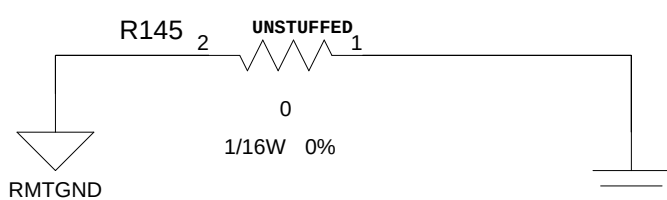


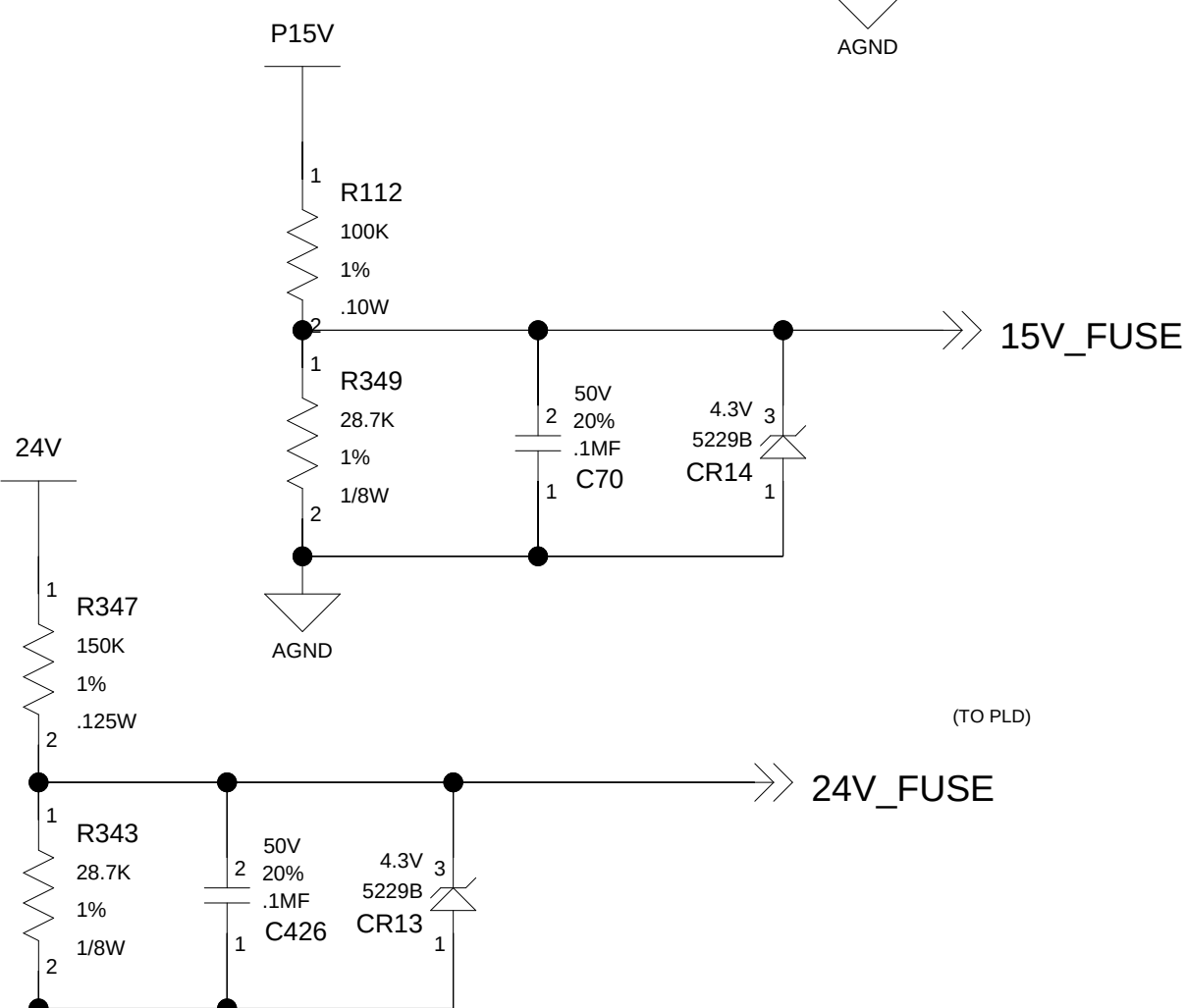
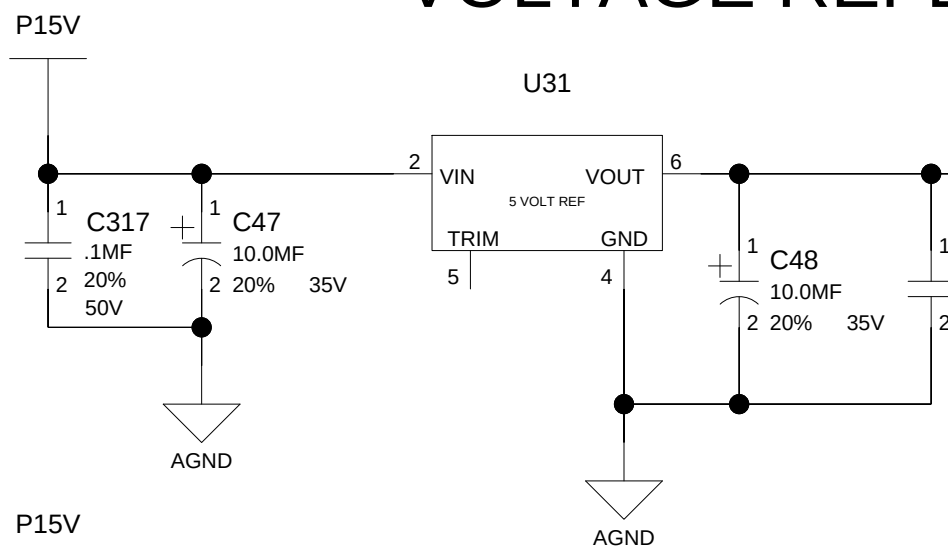
POWER DISTRIBUTION



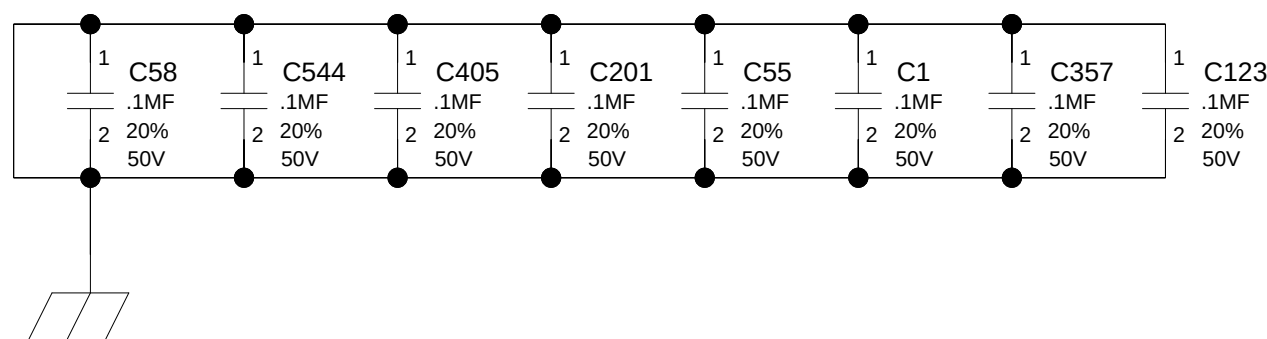
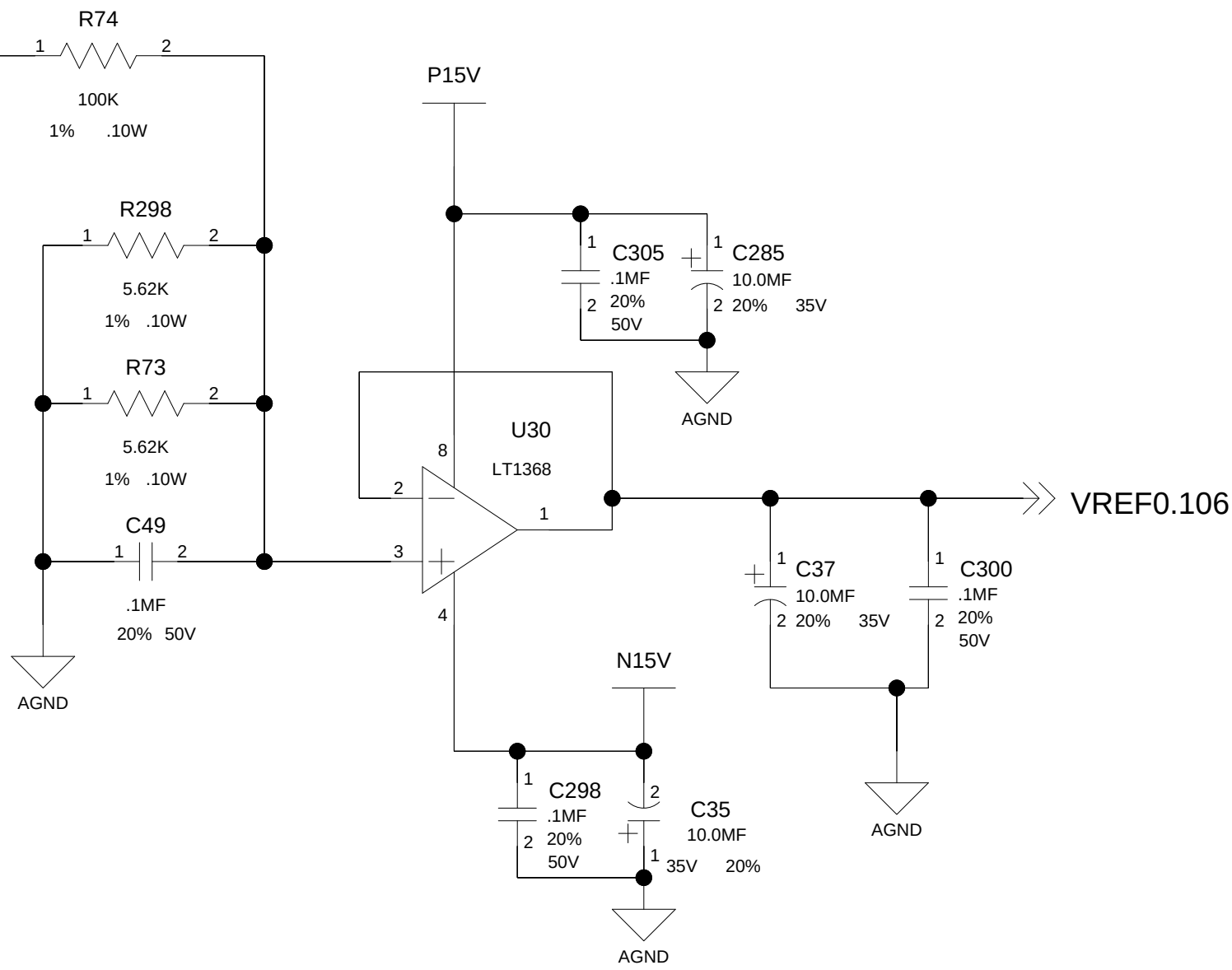
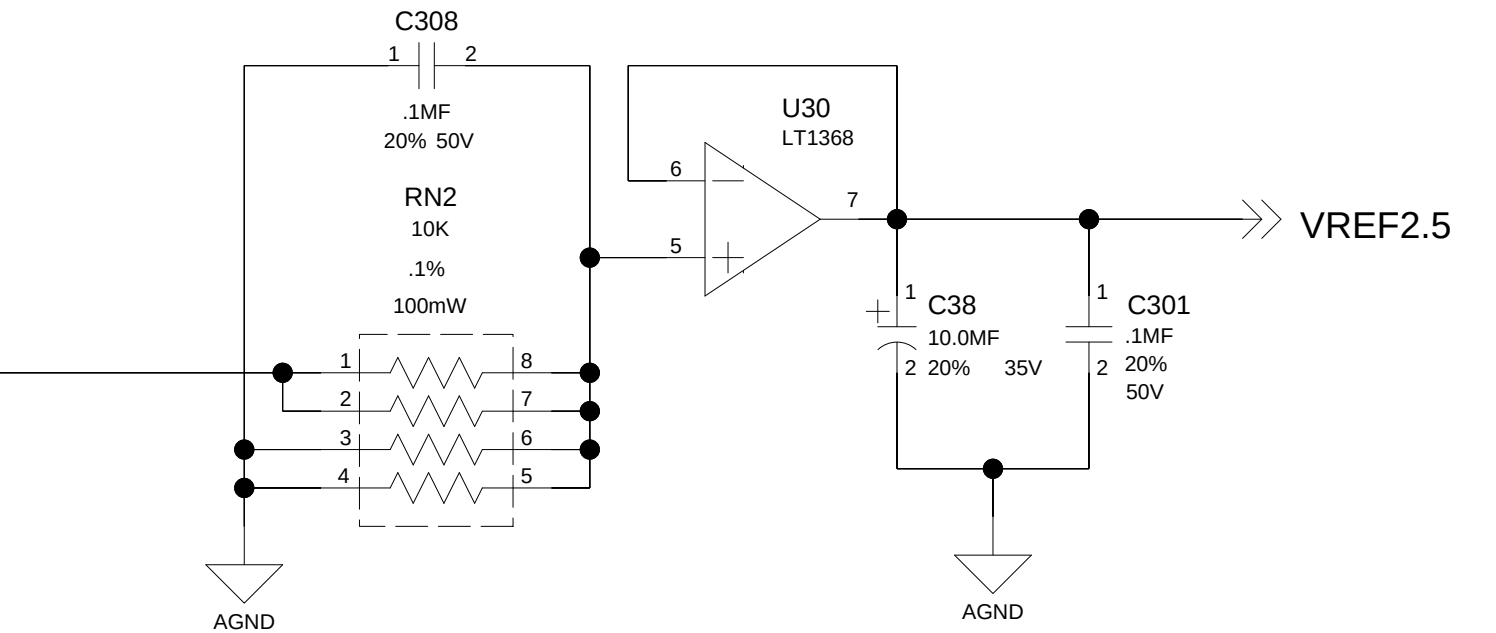
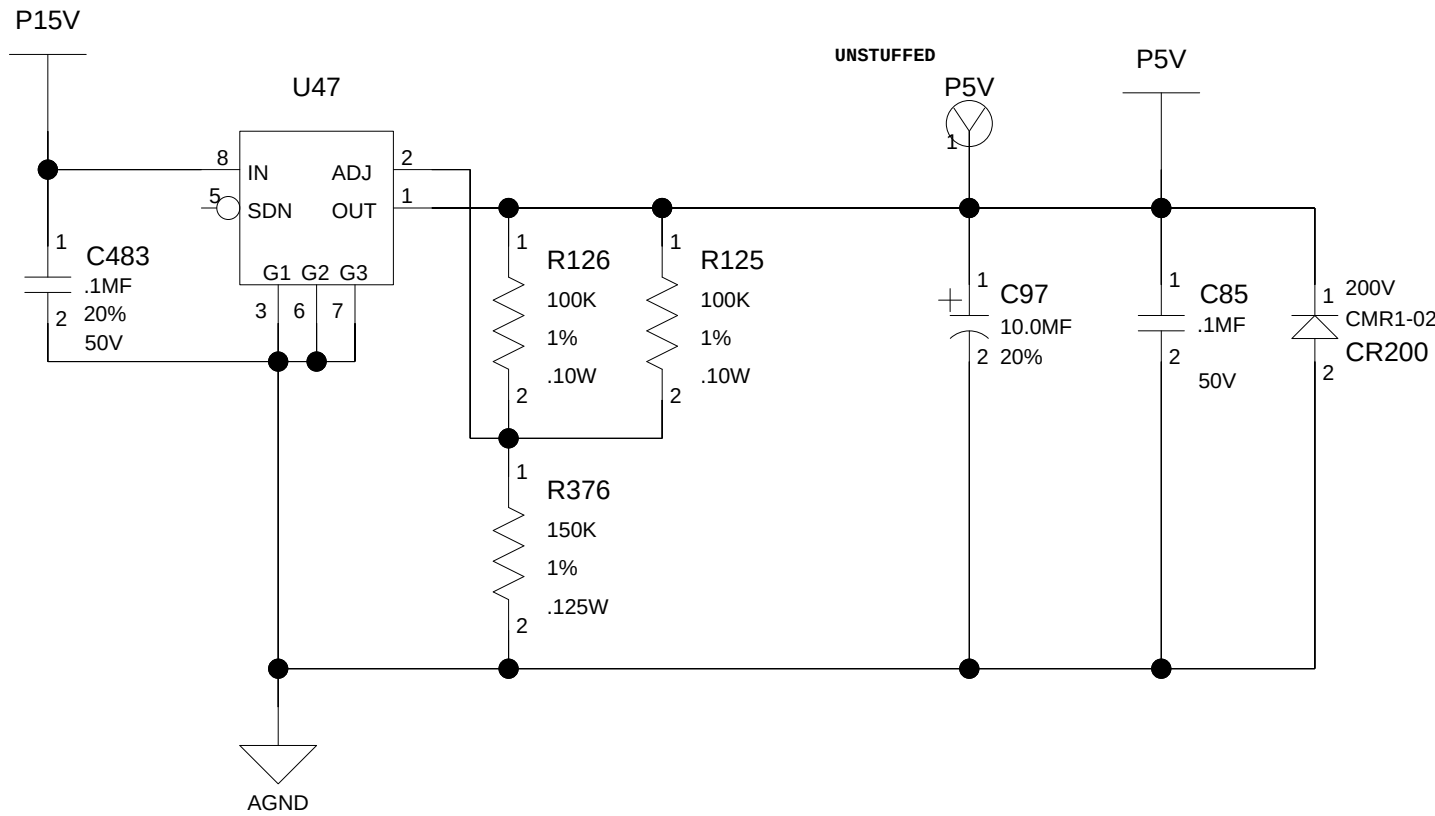
Place Near Power Connector



VOLTAGE REFERENCES



ANALOG 5V SUPPLY



WATERS

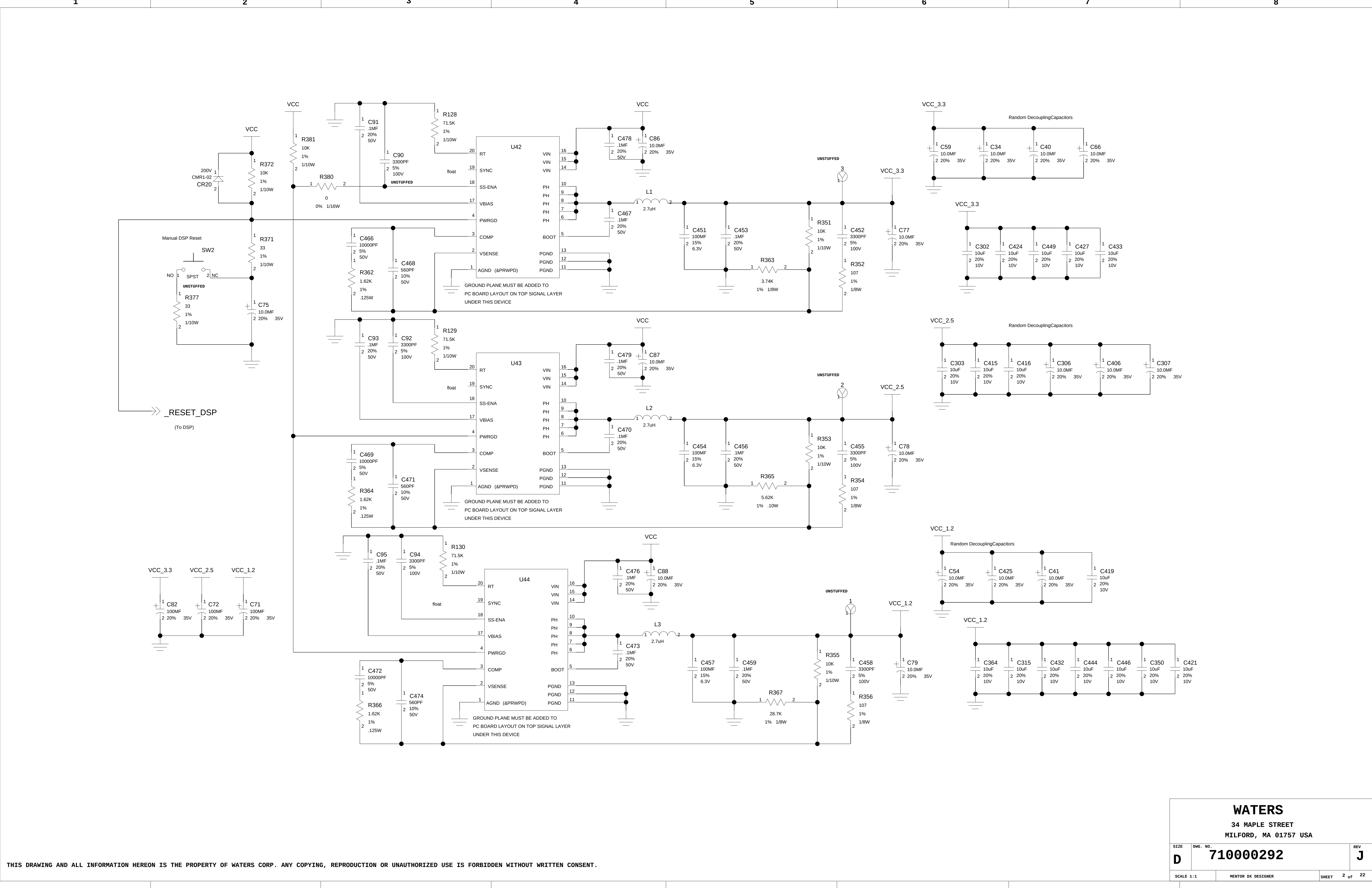
THE SCIENCE OF WHAT'S POSSIBLE
34 MAPLE ST. MILFORD, MA 01757 USA

SCHEM, PCB
2998 CLASSIC PERSONALITY

DRAWN BY	Z. EL-MASSIH
DATE	22-MAY-2014
TIME	13:48:49 UTC
CHANGE NO.	SEE SAP

SIZE	D	DWG NO	710000292	REV	J
SCALE	1:1	MENTOR DX DESIGNER	SHEET	1 of	22

THIS DRAWING AND ALL INFORMATION HEREON IS THE PROPERTY OF WATERS CORP. ANY COPYING, REPRODUCTION OR UNAUTHORIZED USE IS FORBIDDEN WITHOUT WRITTEN CONSENT.



THIS DRAWING AND ALL INFORMATION HEREON IS THE PROPERTY OF WATERS CORP. ANY COPYING, REPRODUCTION OR UNAUTHORIZED USE IS FORBIDDEN WITHOUT WRITTEN CONSENT.

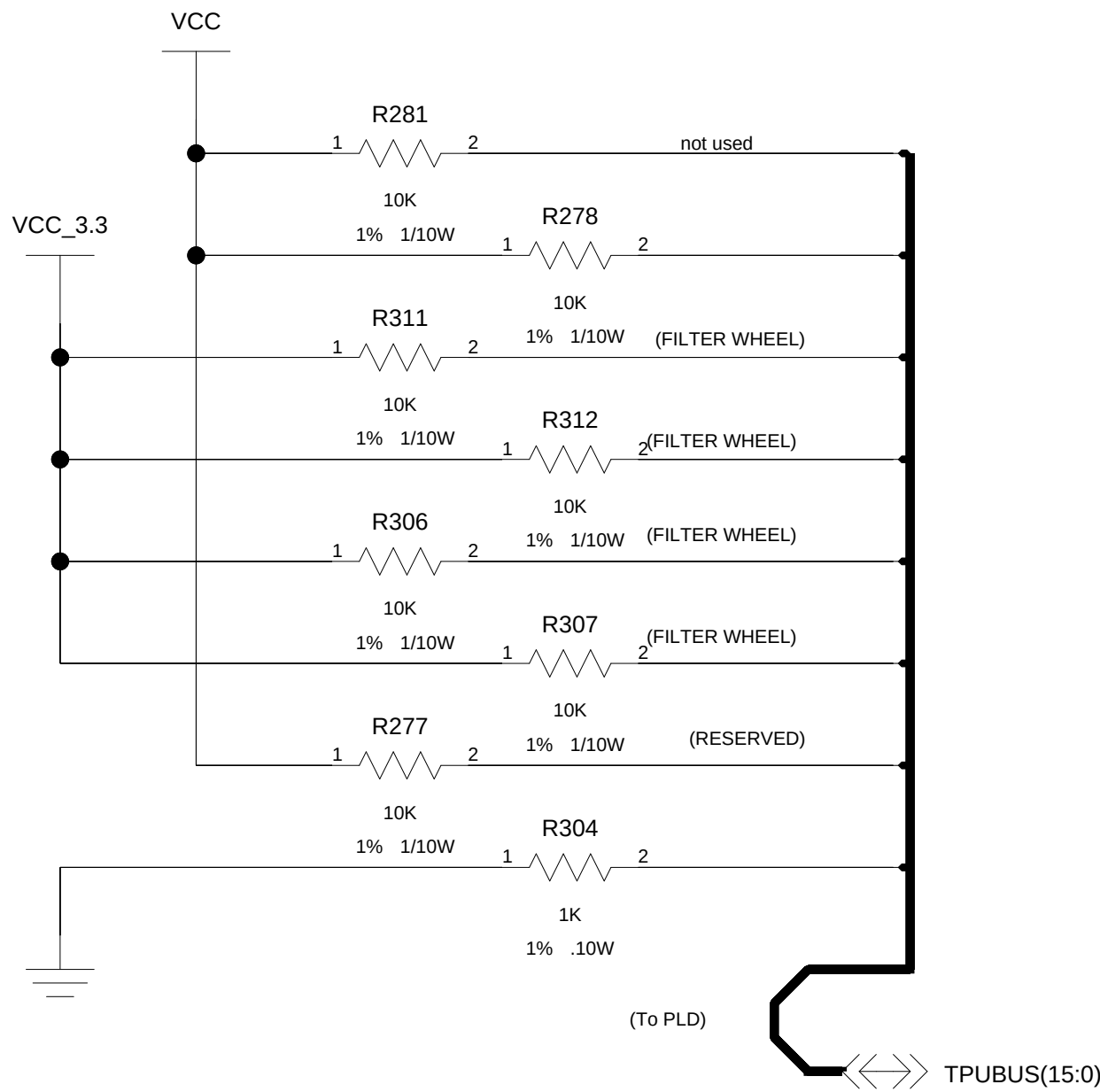
WATERS

34 MAPLE STREET

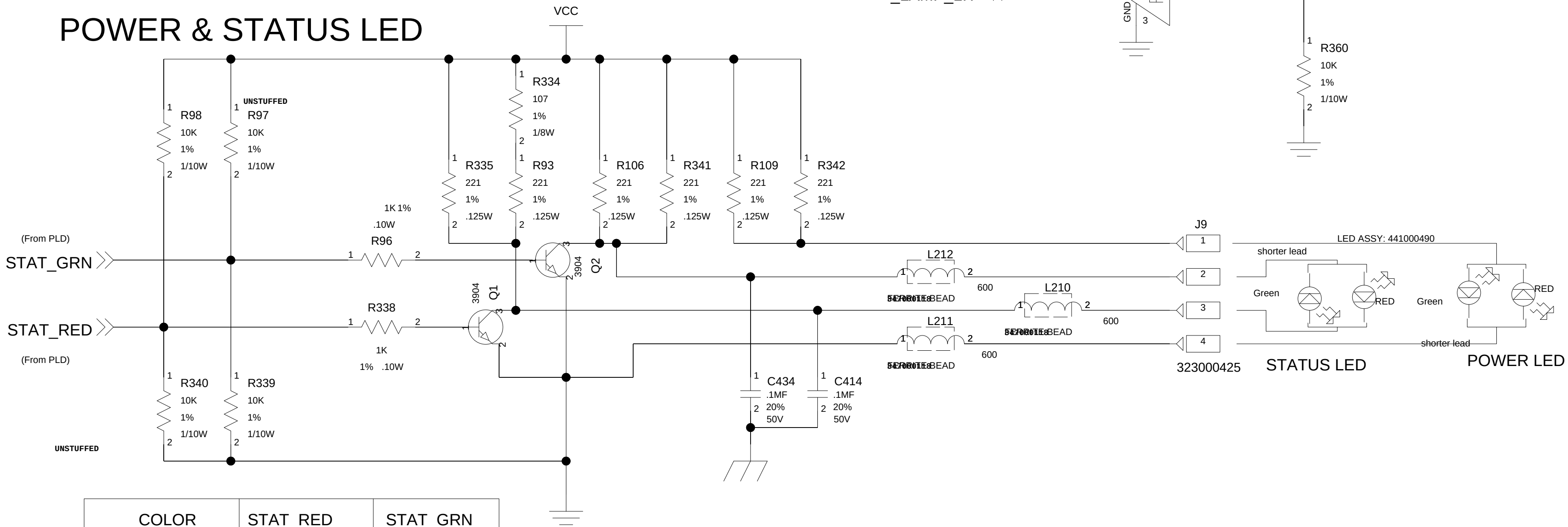
MILFORD, MA 01757 USA

SIZE	DWG. NO.	REV
D	710000292	J
SCALE 1:1		SHEET 2 of 22

TPUBUS CHANNELS TO FPGA

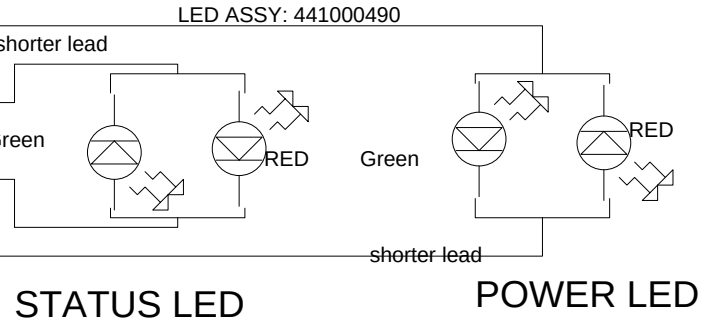
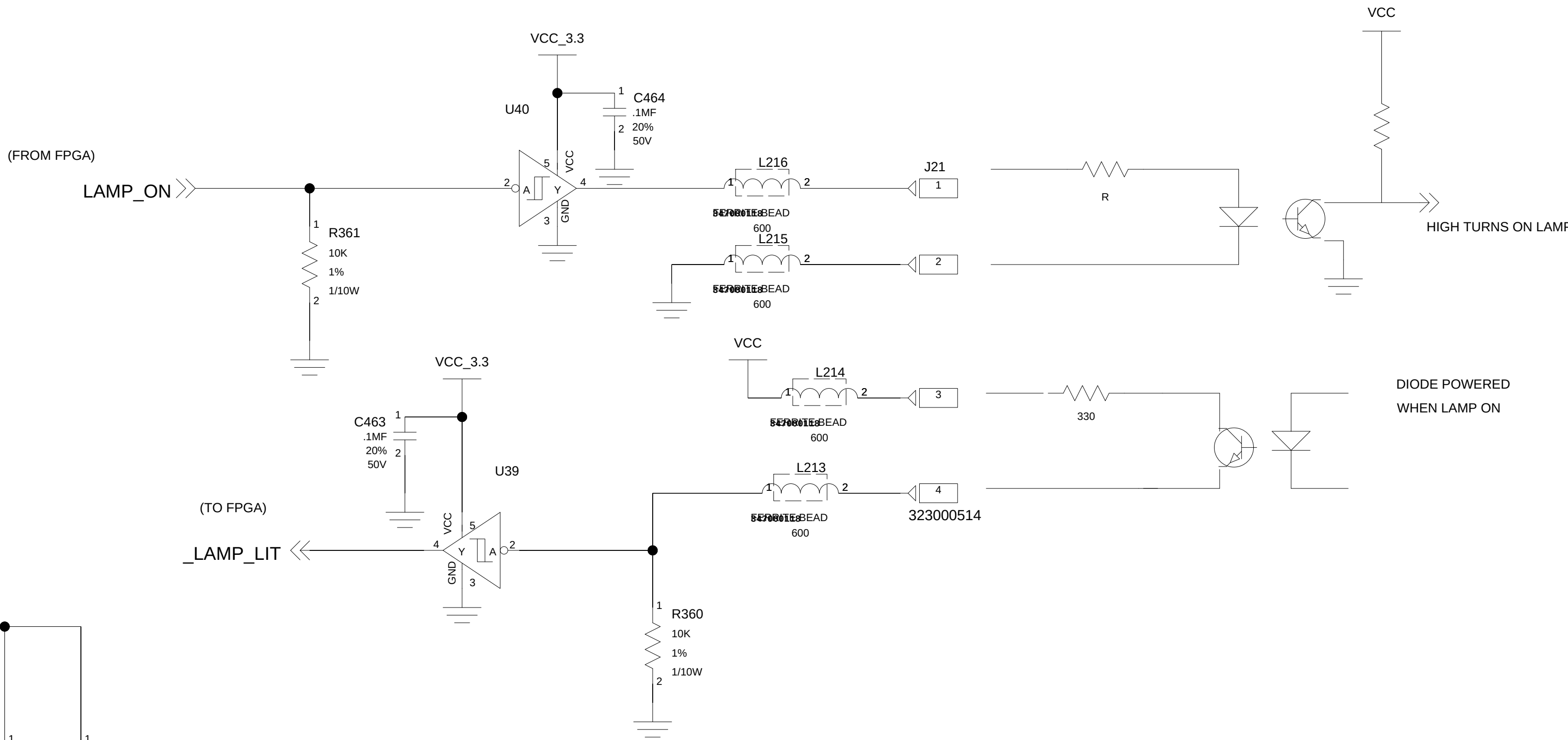


POWER & STATUS LED

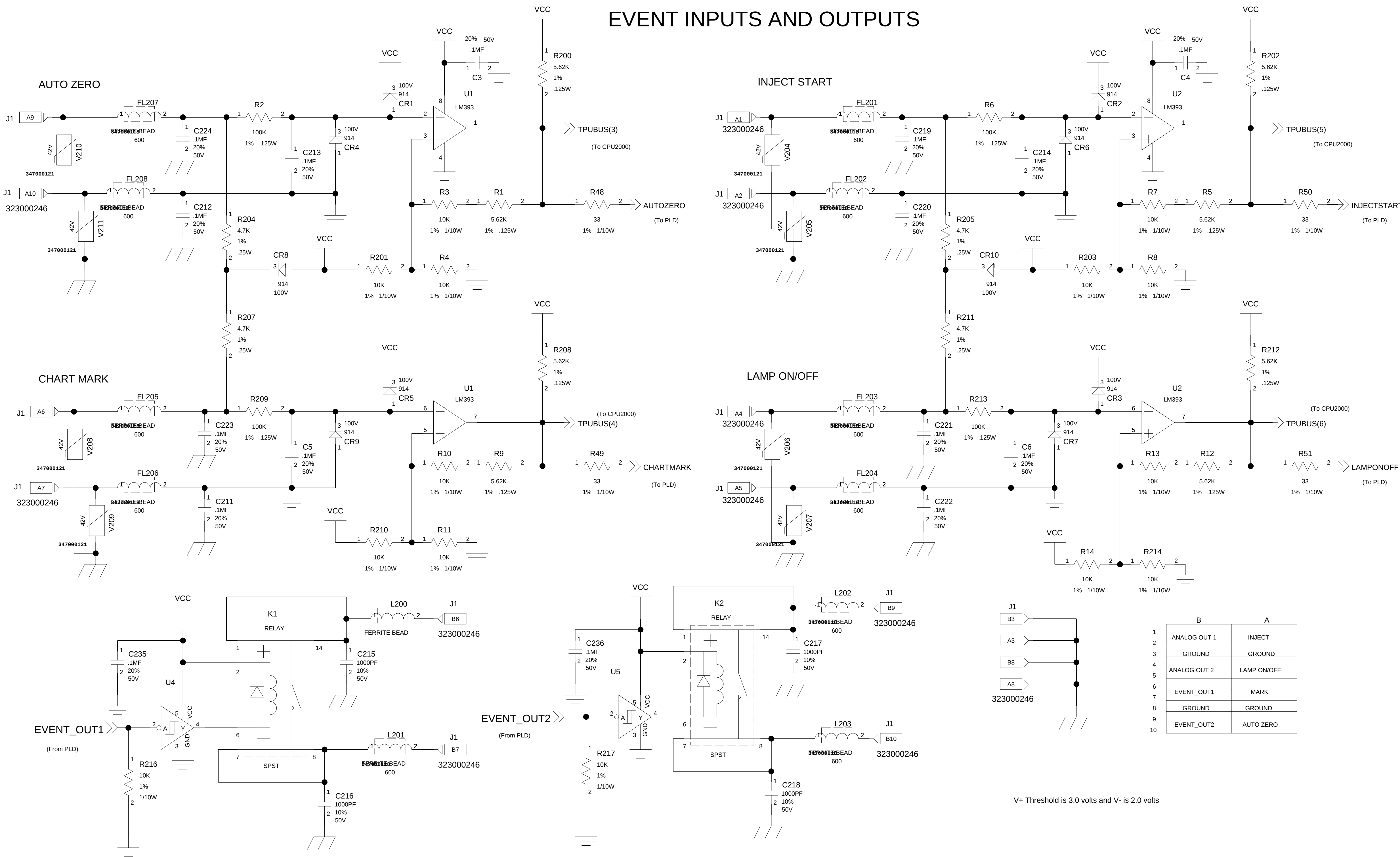


COLOR	STAT_RED	STAT_GRN
Off	0	0
Green	0	1
RED	1	0
Not allowed	1	1

HB LAMP POWER SUPPLY



EVENT INPUTS AND OUTPUTS



WATERS

34 MAPLE STREET
MILFORD, MA 01757 USA

SIZE

DWG. NO.

D

710000292

REV

J

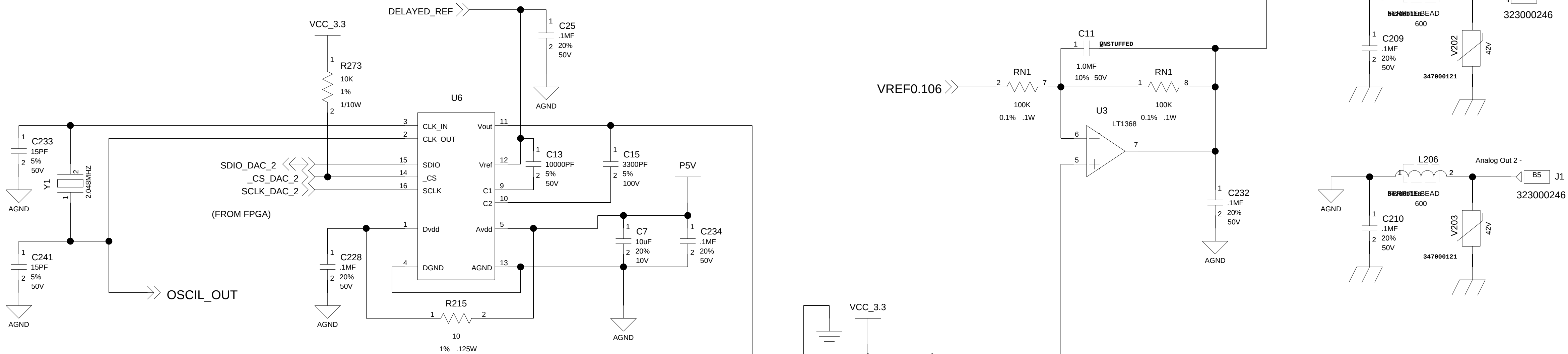
SCALE 1:1

MENTOR DX DESIGNER

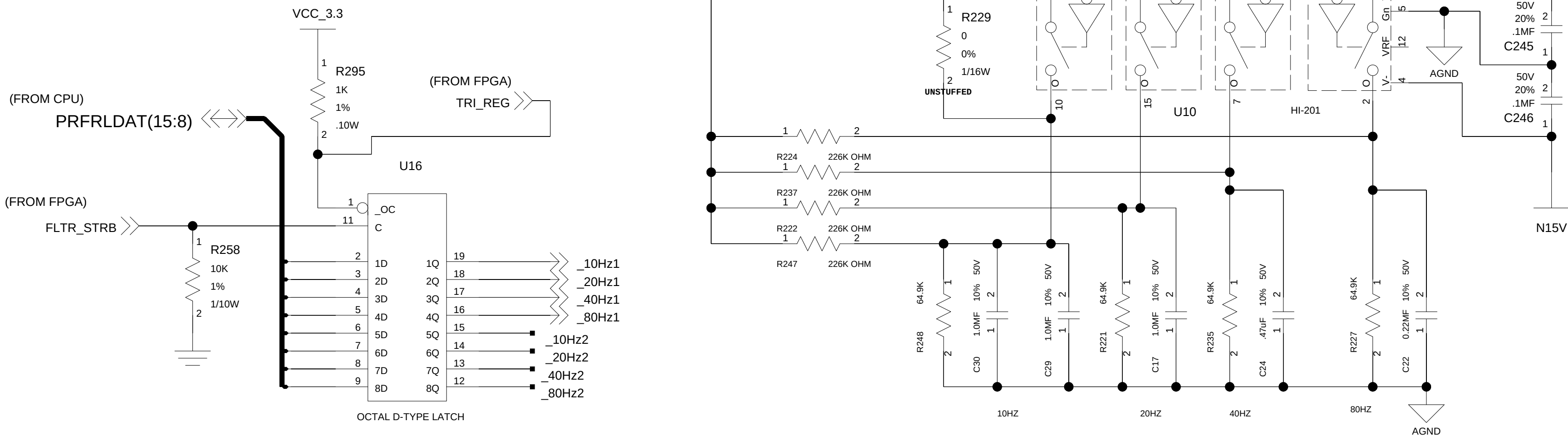
SHEET

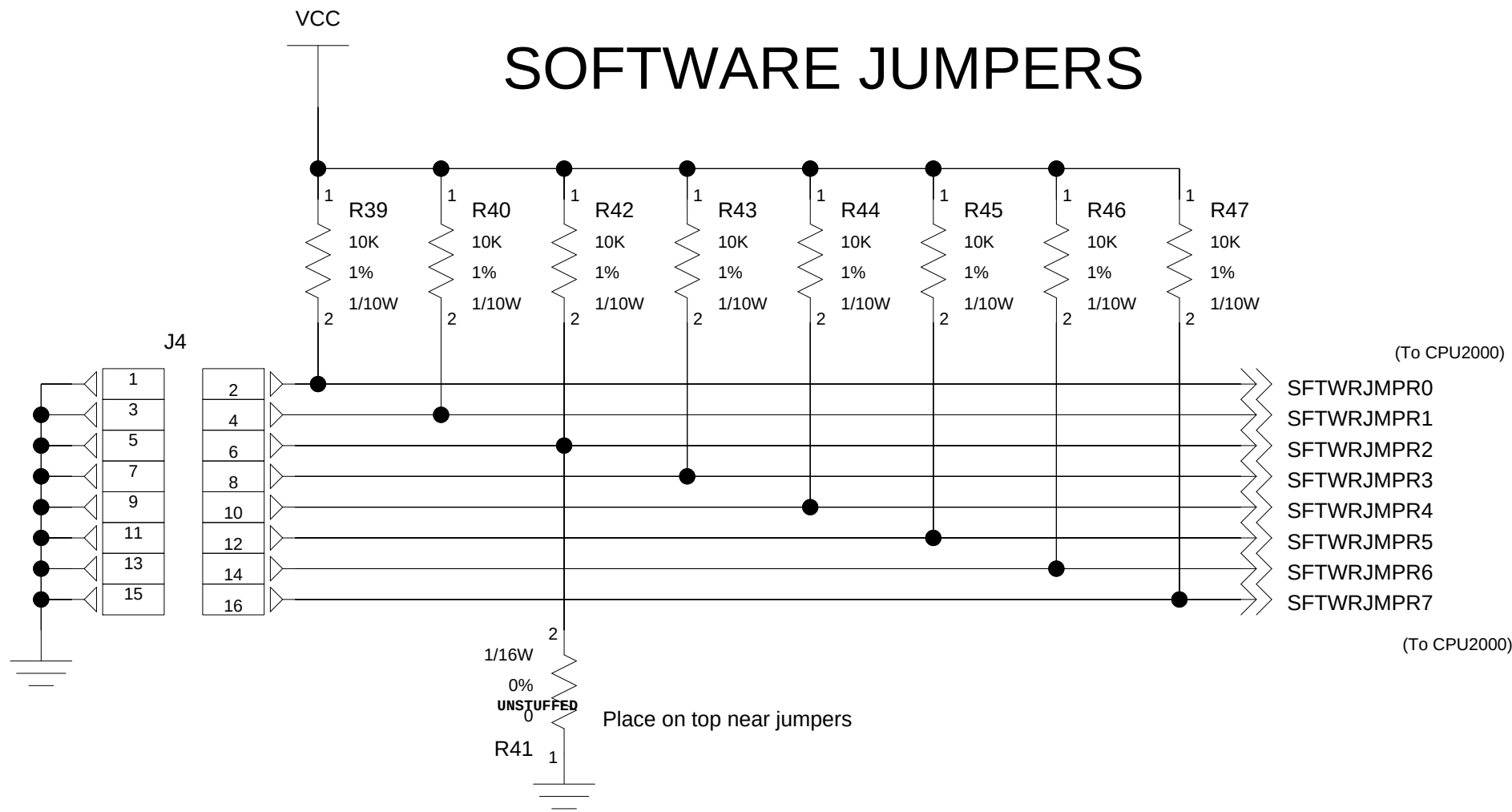
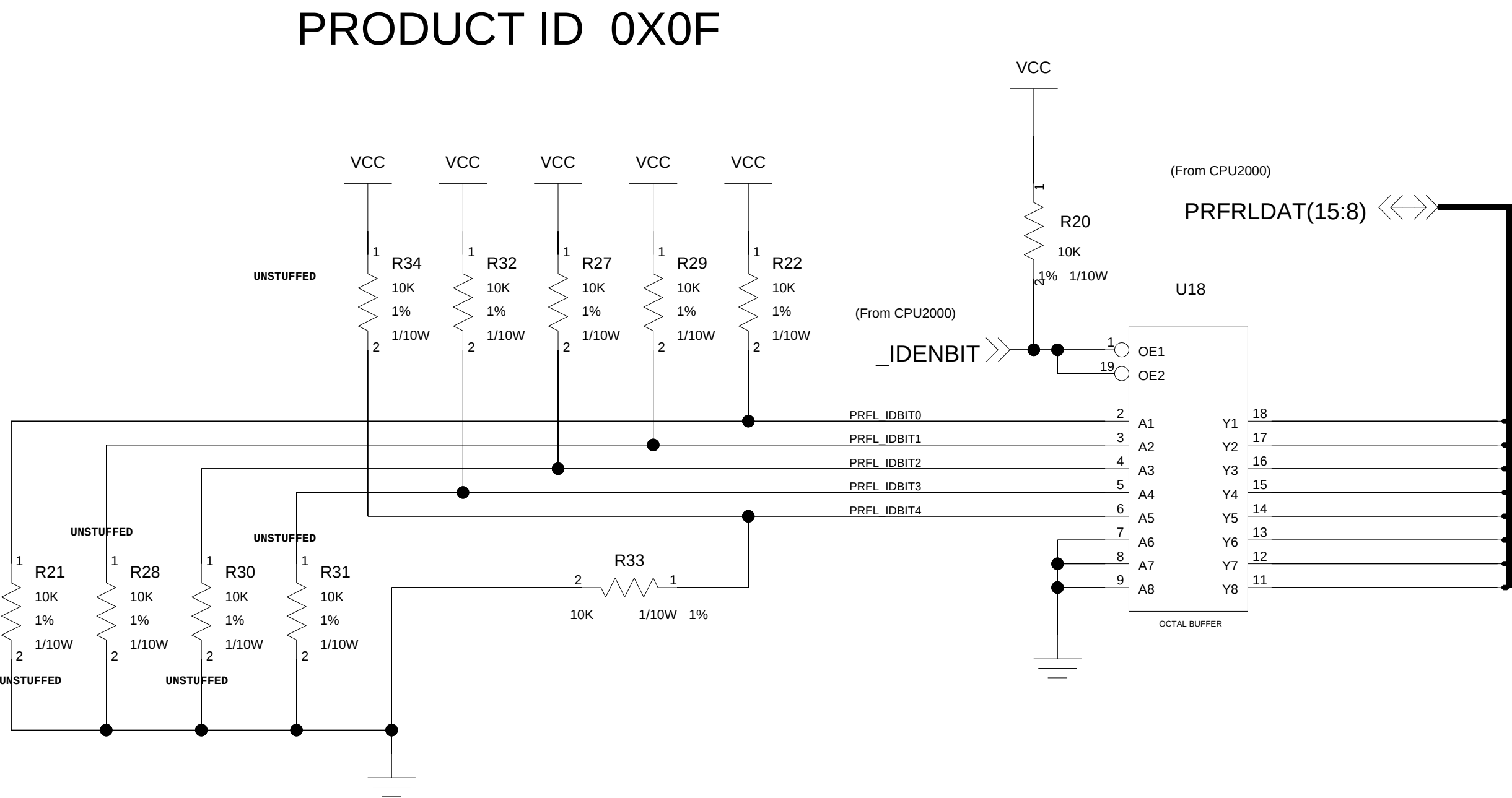
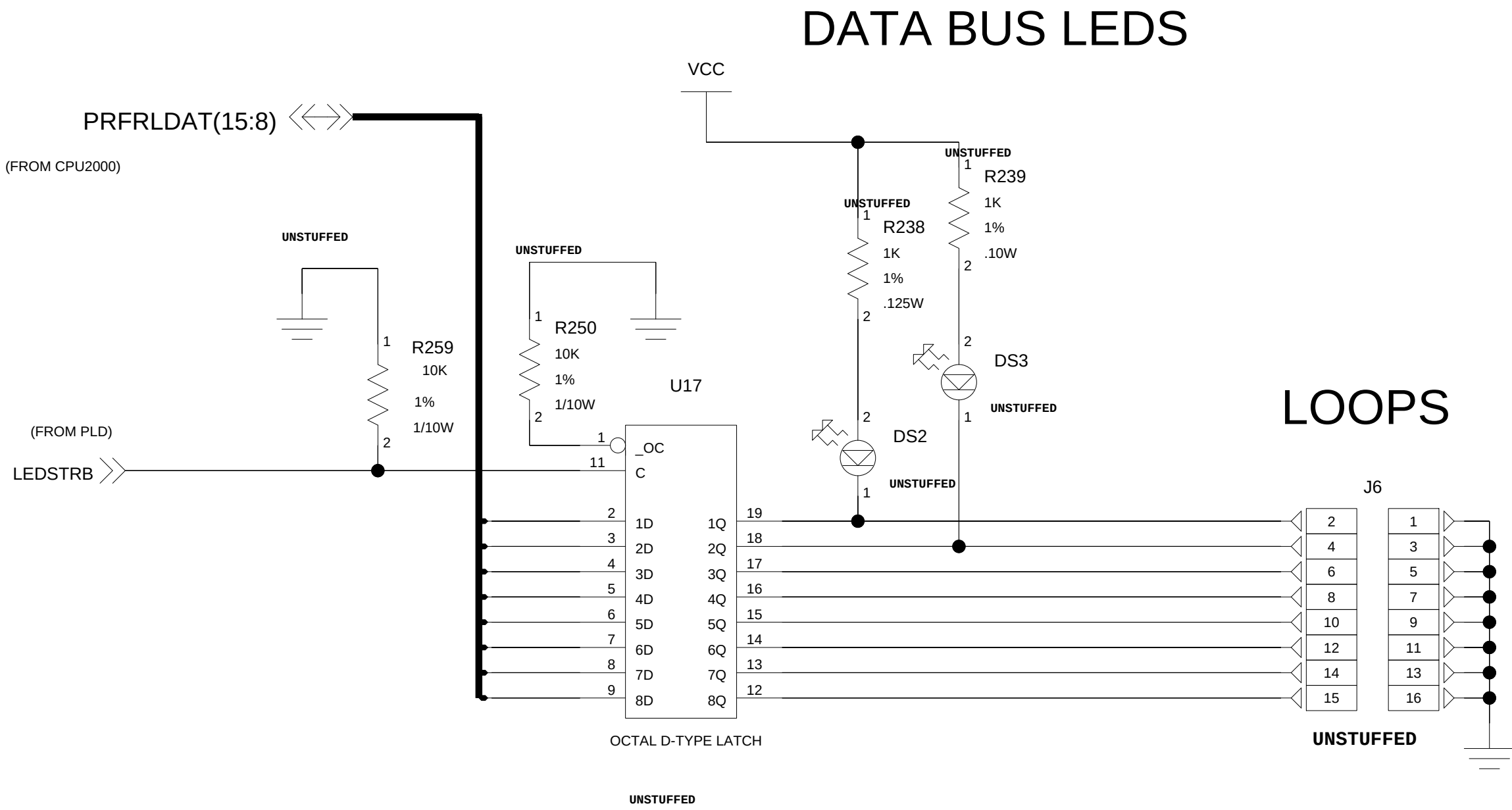
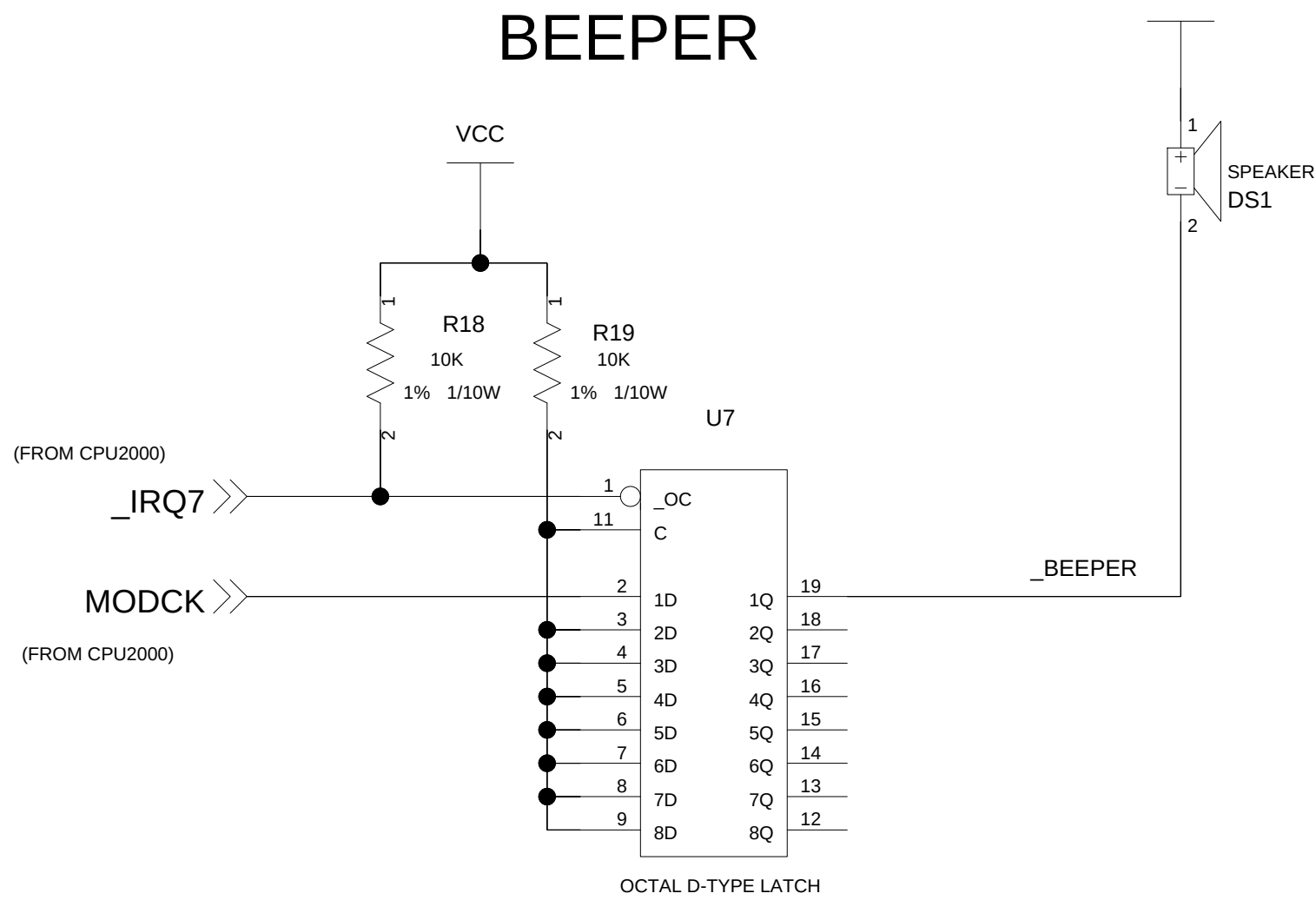
4 of 22

Analog Output CH2 -0.1 to 2.1 Volts

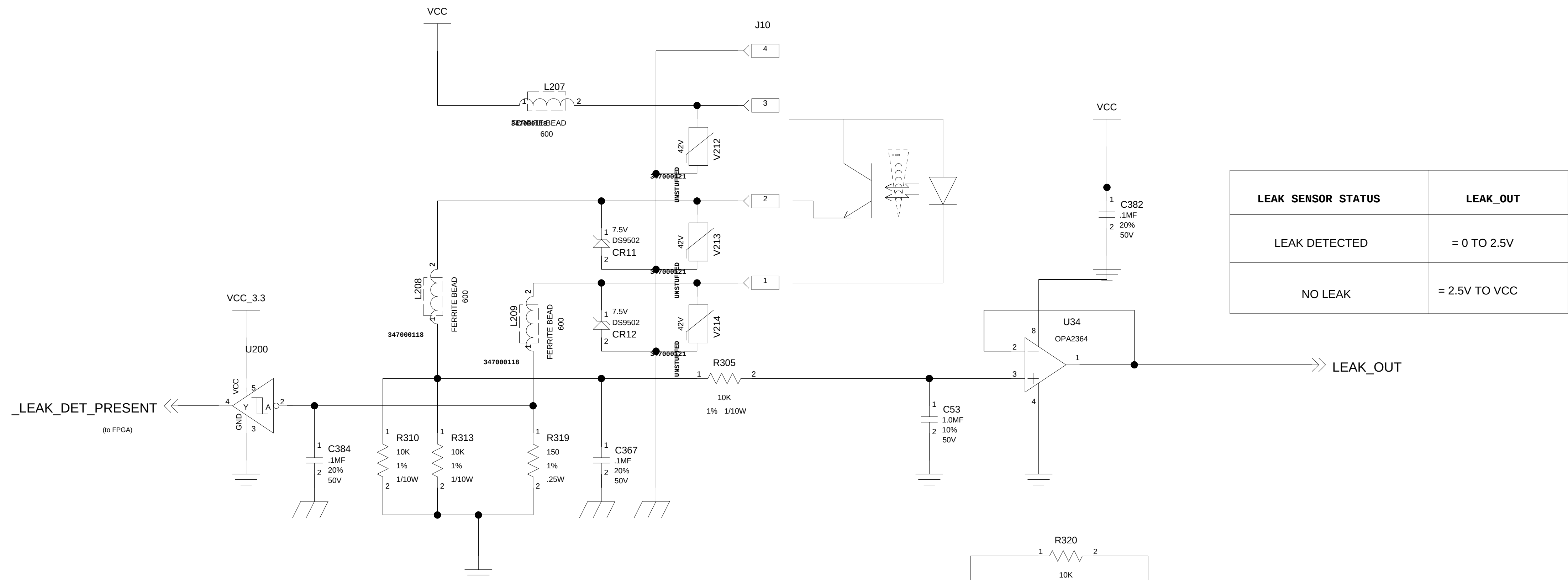


WRITE REGISTER

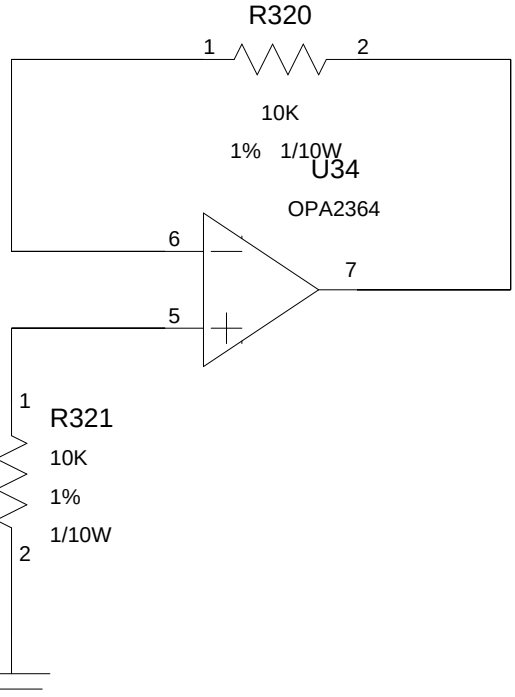
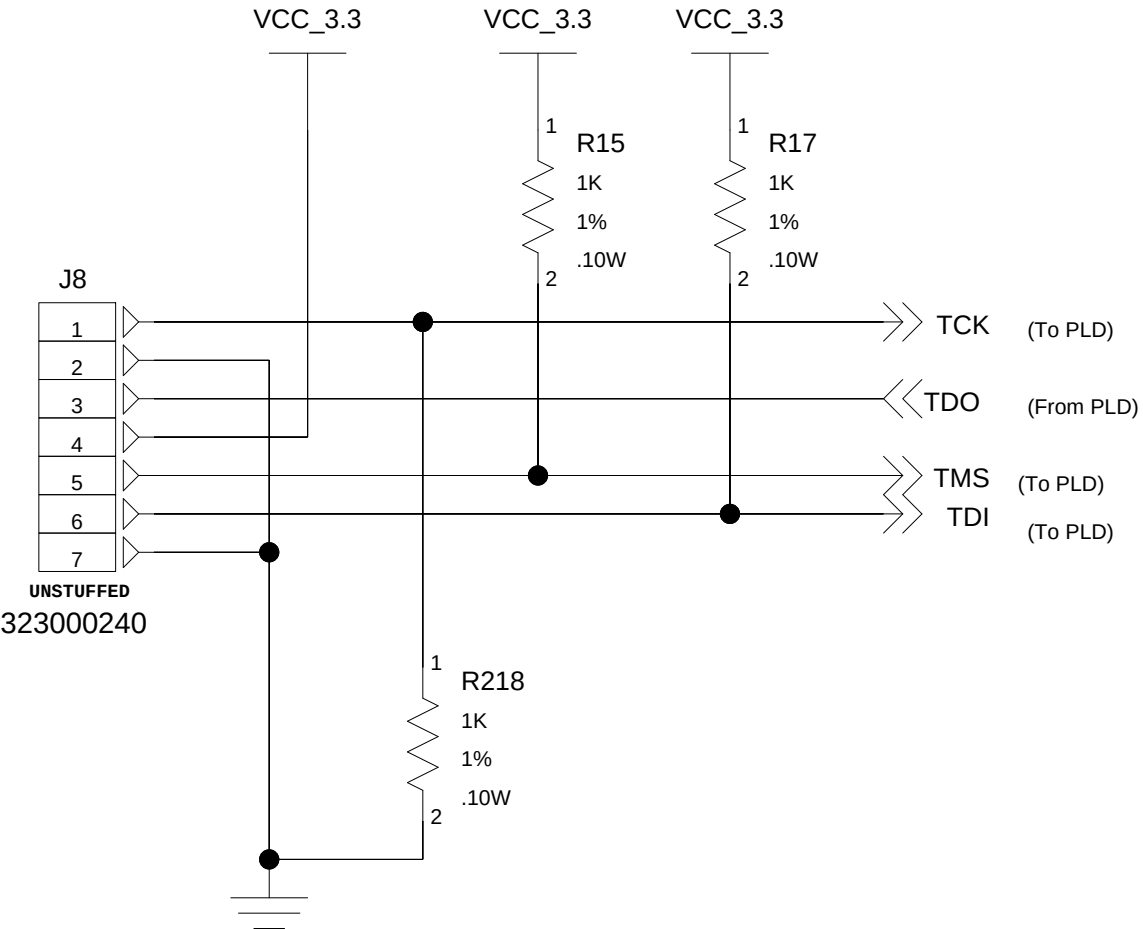




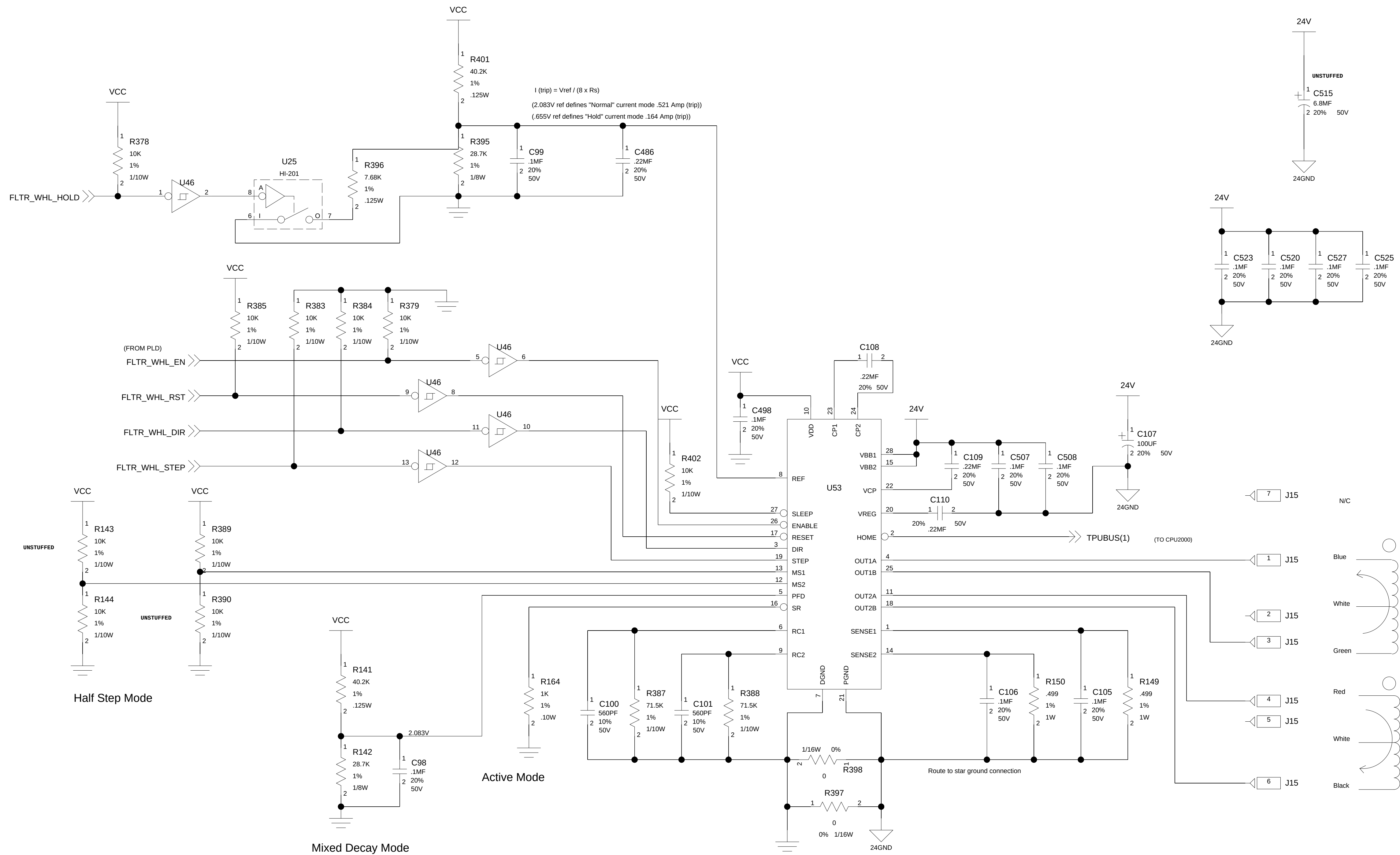
Leak Detector Circuit



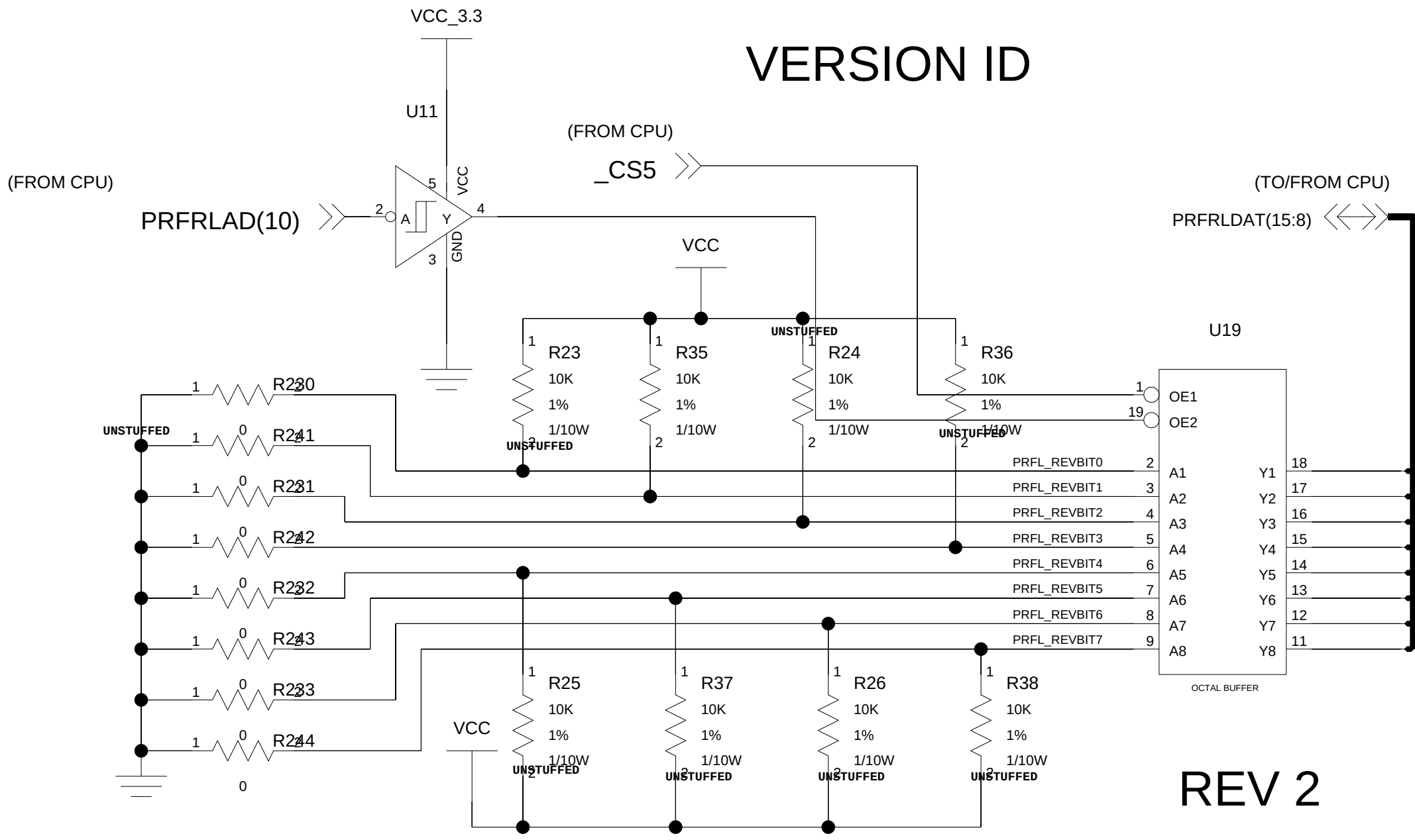
FPGA JTAG CONNECTOR

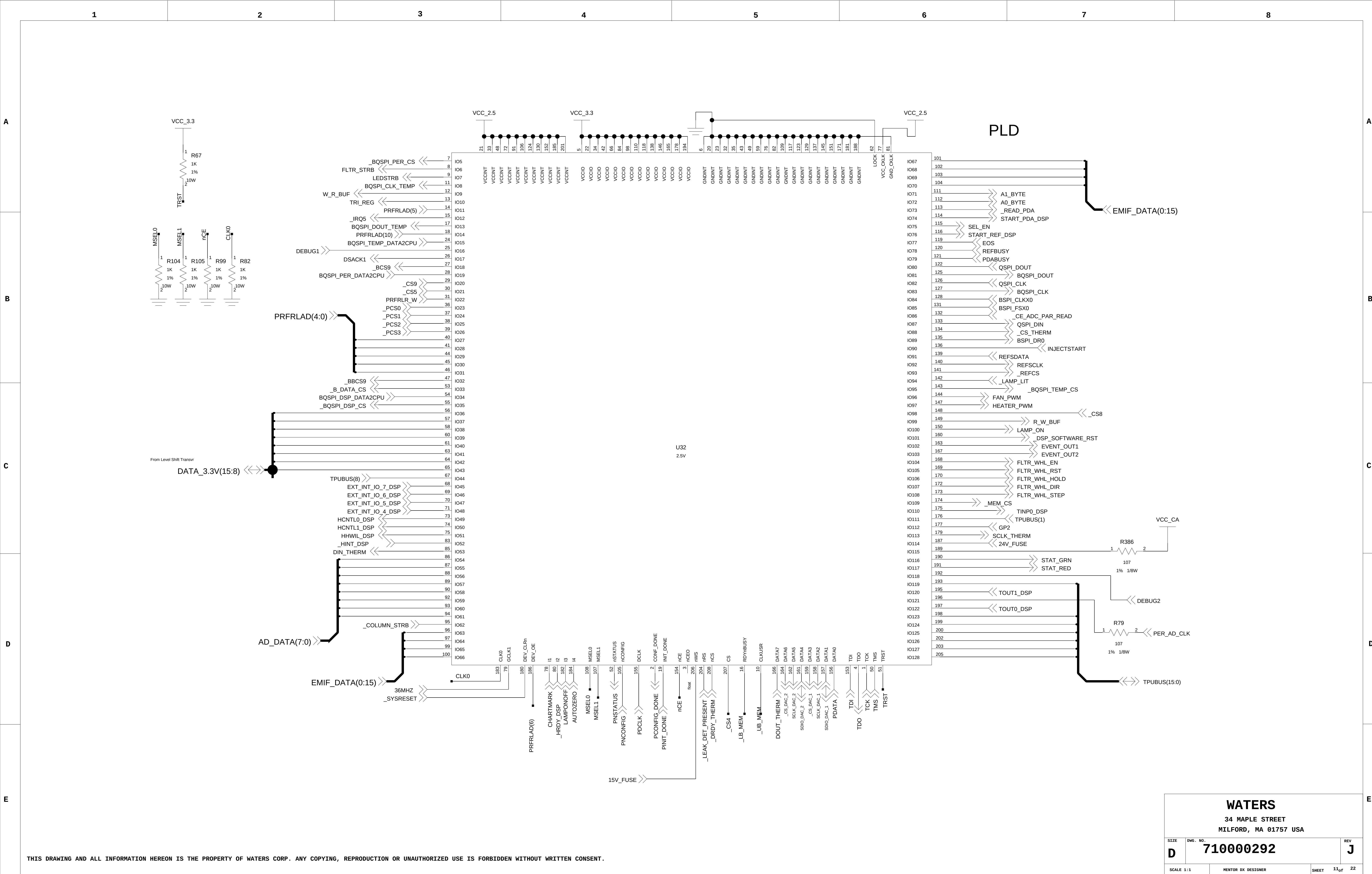


FILTER WHEEL DRIVER



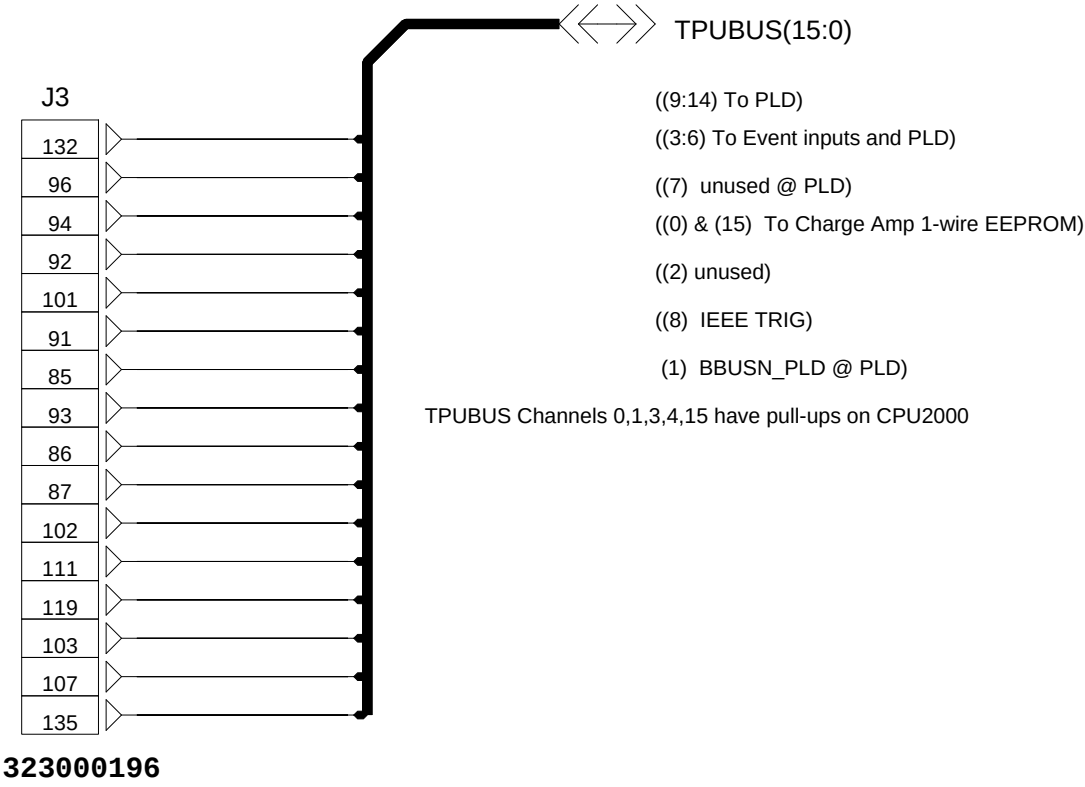
THIS DRAWING AND ALL INFORMATION HEREON IS THE PROPERTY OF WATERS CORP. ANY COPYING, REPRODUCTION OR UNAUTHORIZED USE IS FORBIDDEN WITHOUT WRITTEN CONSENT.



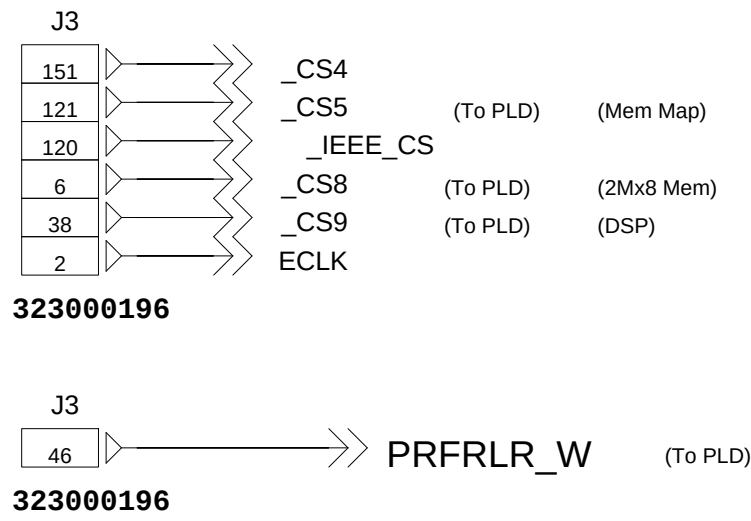


CPU2000 CONNECTOR

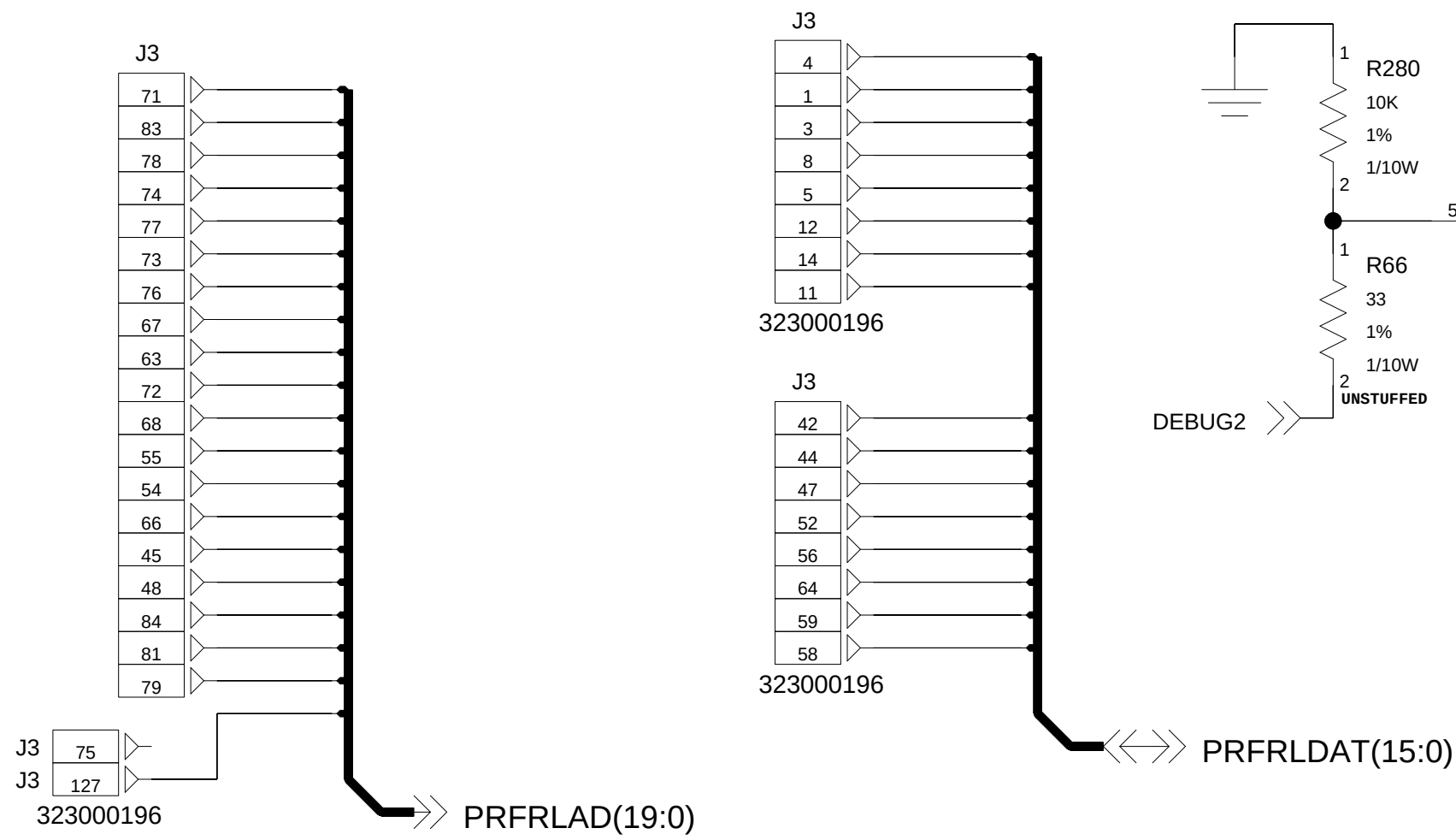
TPUBUS INTERFACE



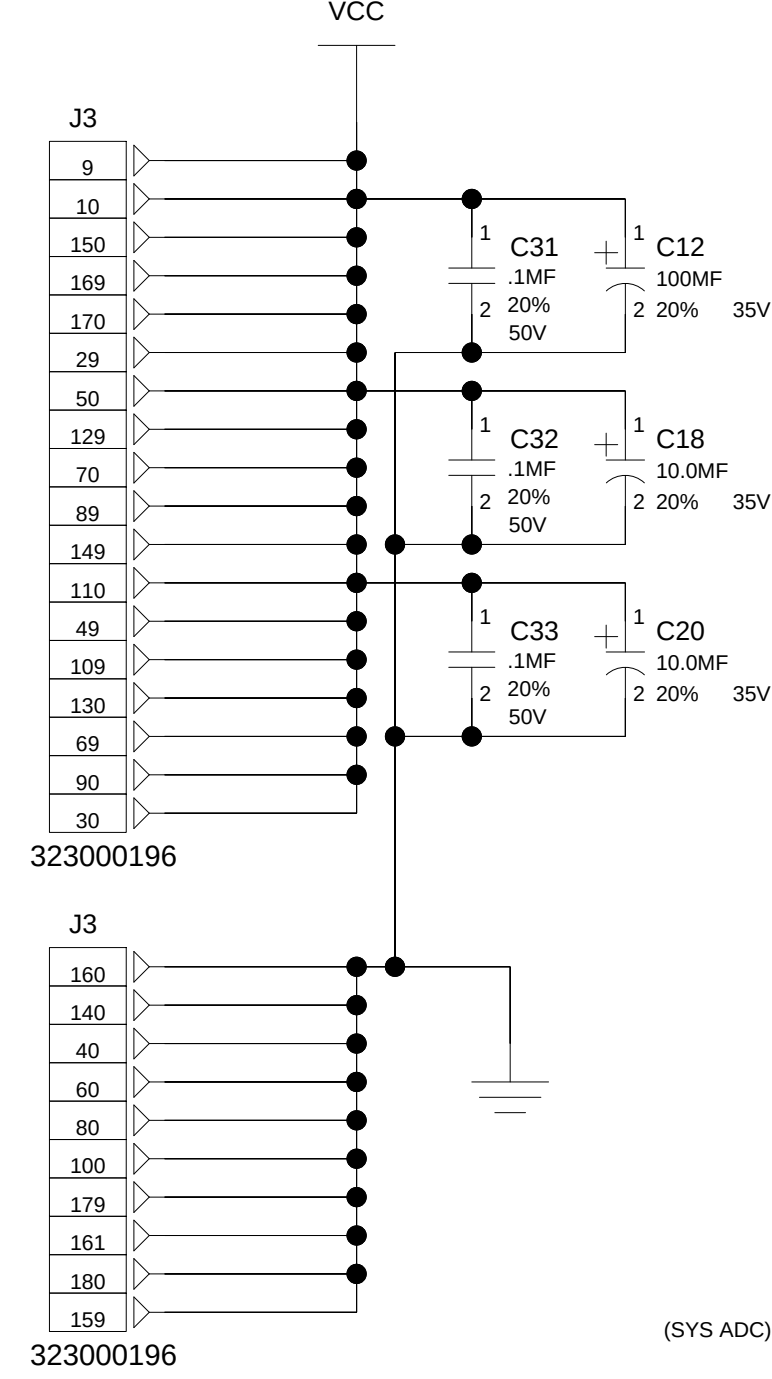
CHIP SELECT & R/W INTERFACE



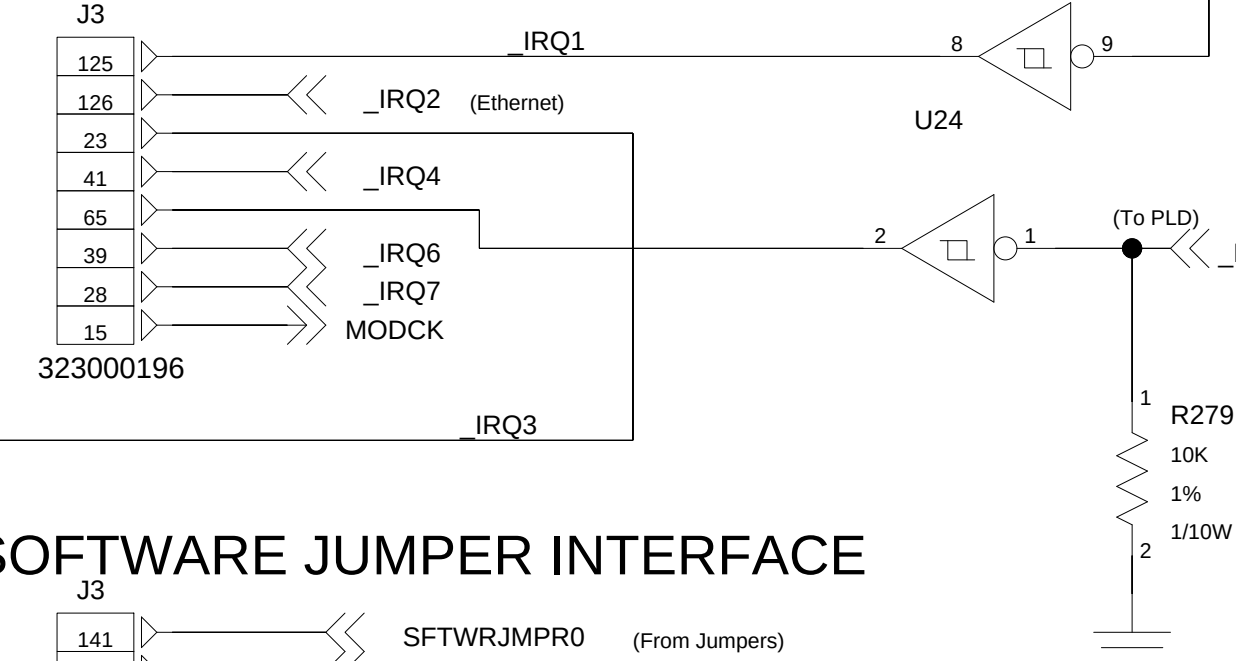
DATA & ADDRESS INTERFACE



POWER INTERFACE



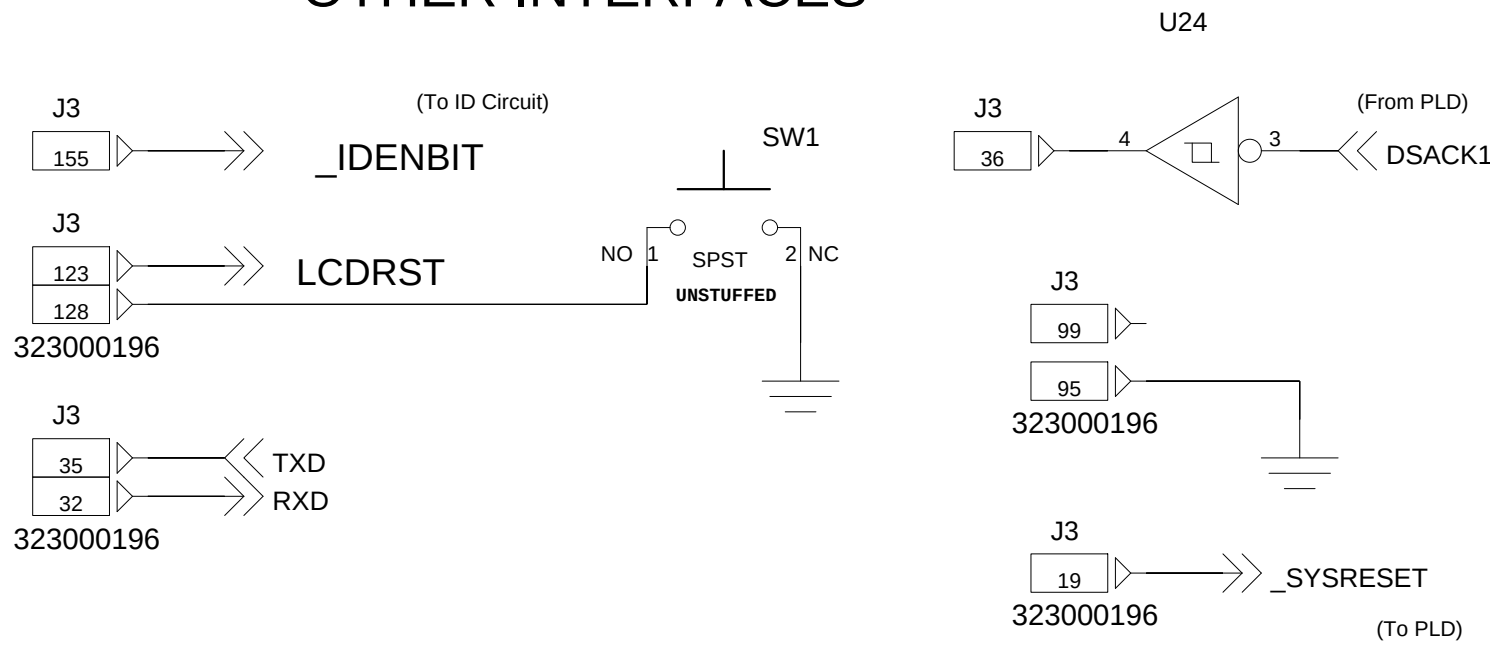
INTERUPTS INTERFACE



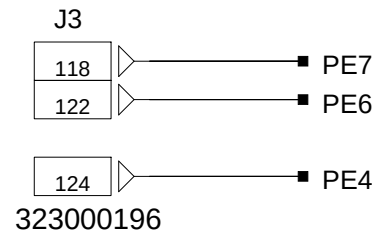
SOFTWARE JUMPER INTERFACE



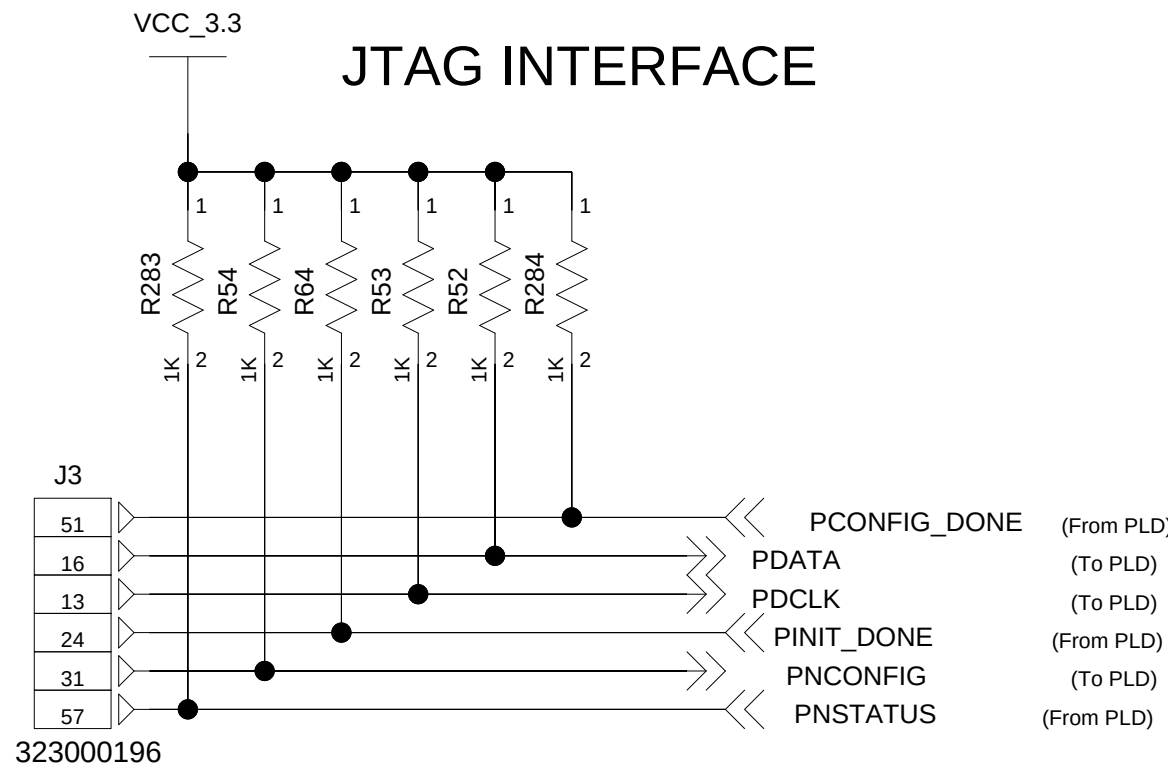
OTHER INTERFACES



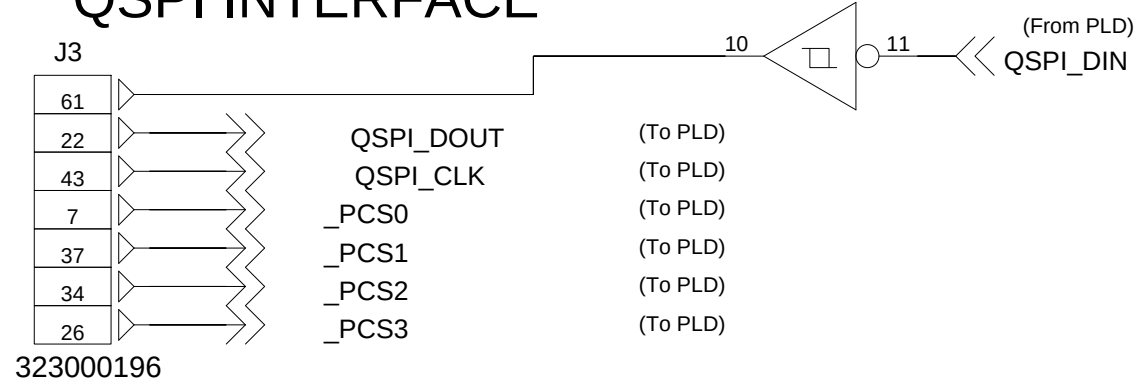
I/O PORTS INTERFACE



JTAG INTERFACE



QSPI INTERFACE



WATERS

34 MAPLE STREET
MILFORD, MA 01757 USA

SIZE

D

DWG. NO.

710000292

REV

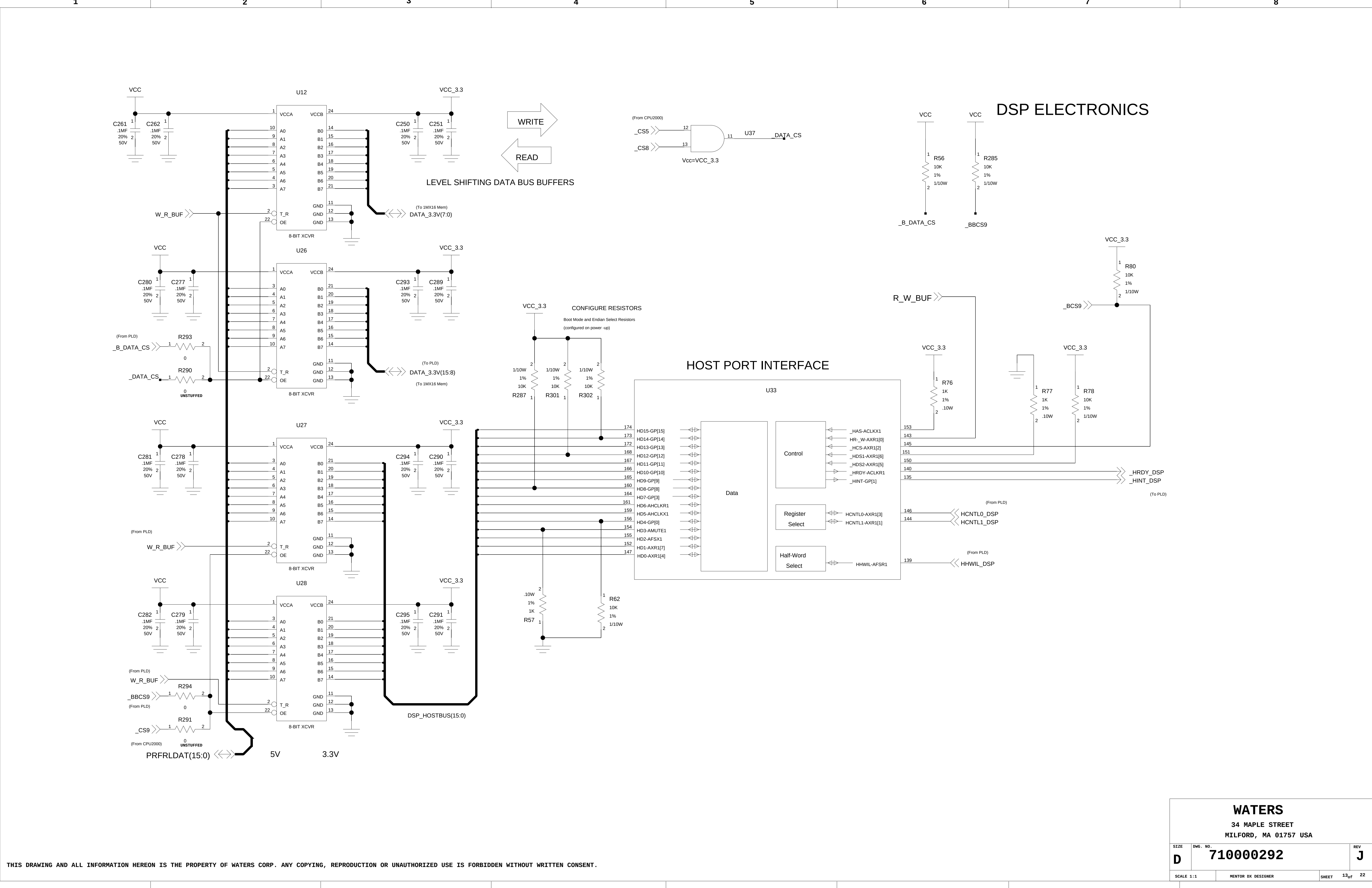
J

SCALE 1:1

MENTOR DX DESIGNER

SHEET

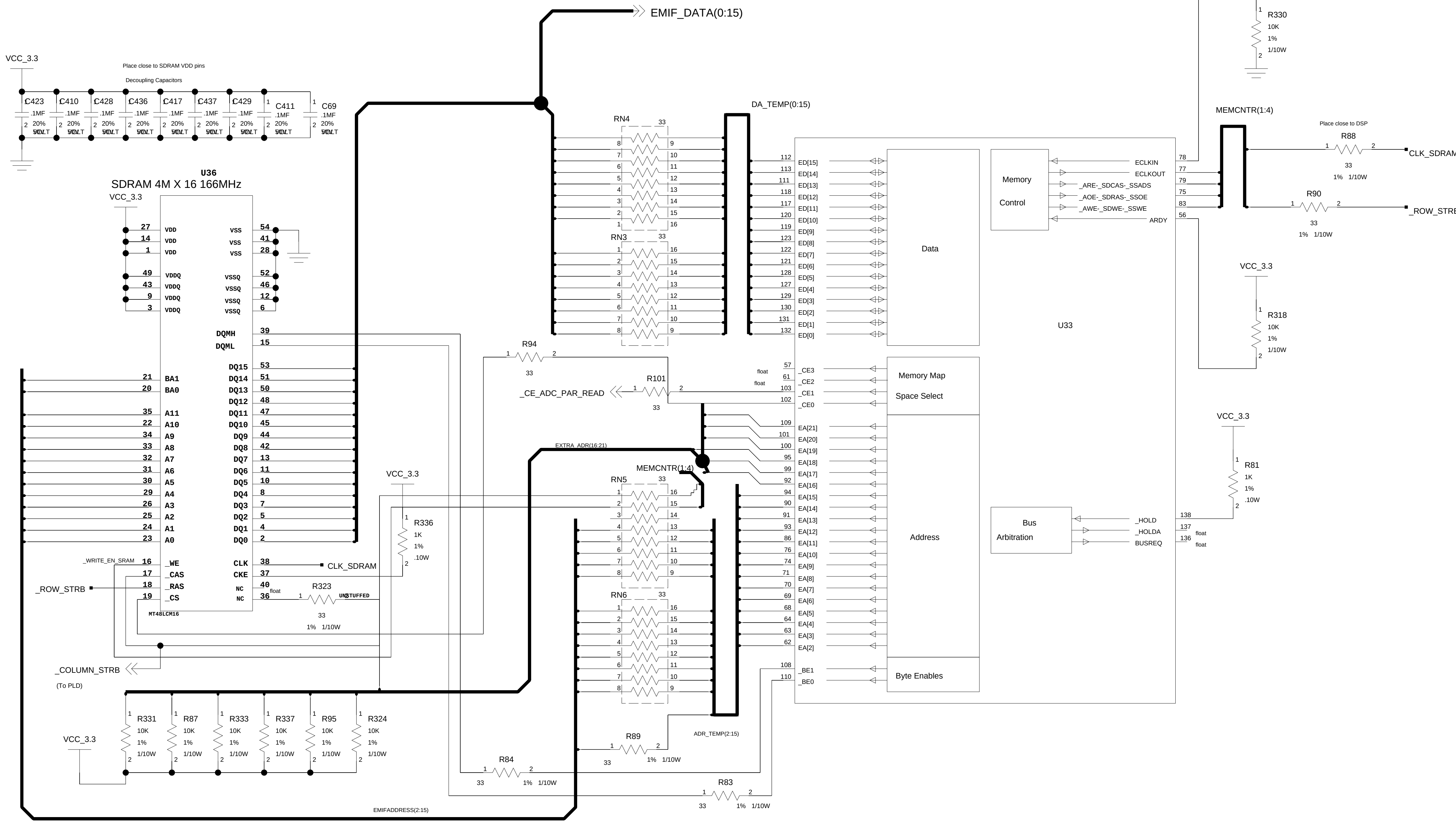
12 of 22

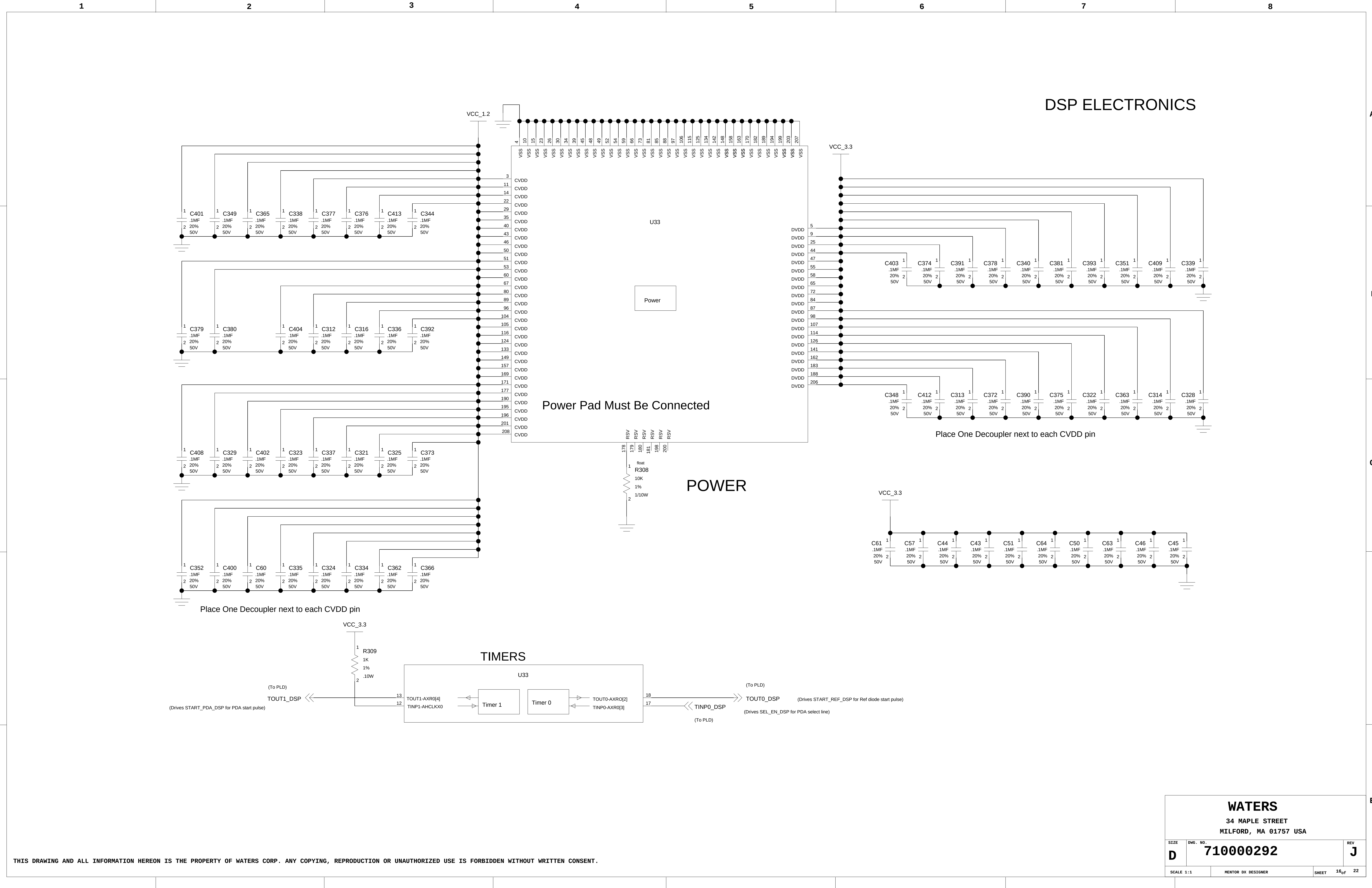


THIS DRAWING AND ALL INFORMATION HEREON IS THE PROPERTY OF WATERS CORP. ANY COPYING, REPRODUCTION OR UNAUTHORIZED USE IS FORBIDDEN WITHOUT WRITTEN CONSENT.

EXTERNAL MEMORY INTERFACE

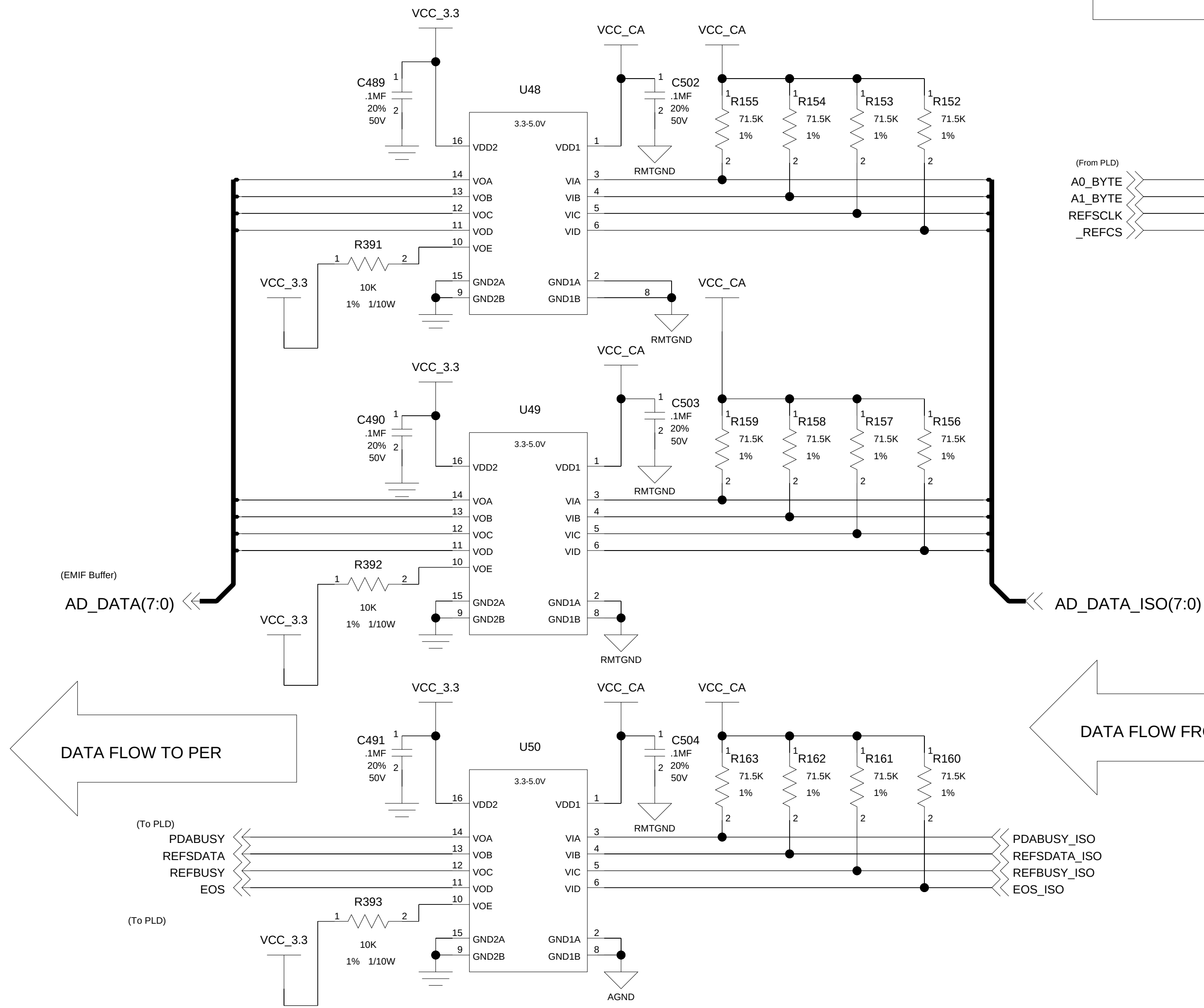
DSP ELECTRONICS



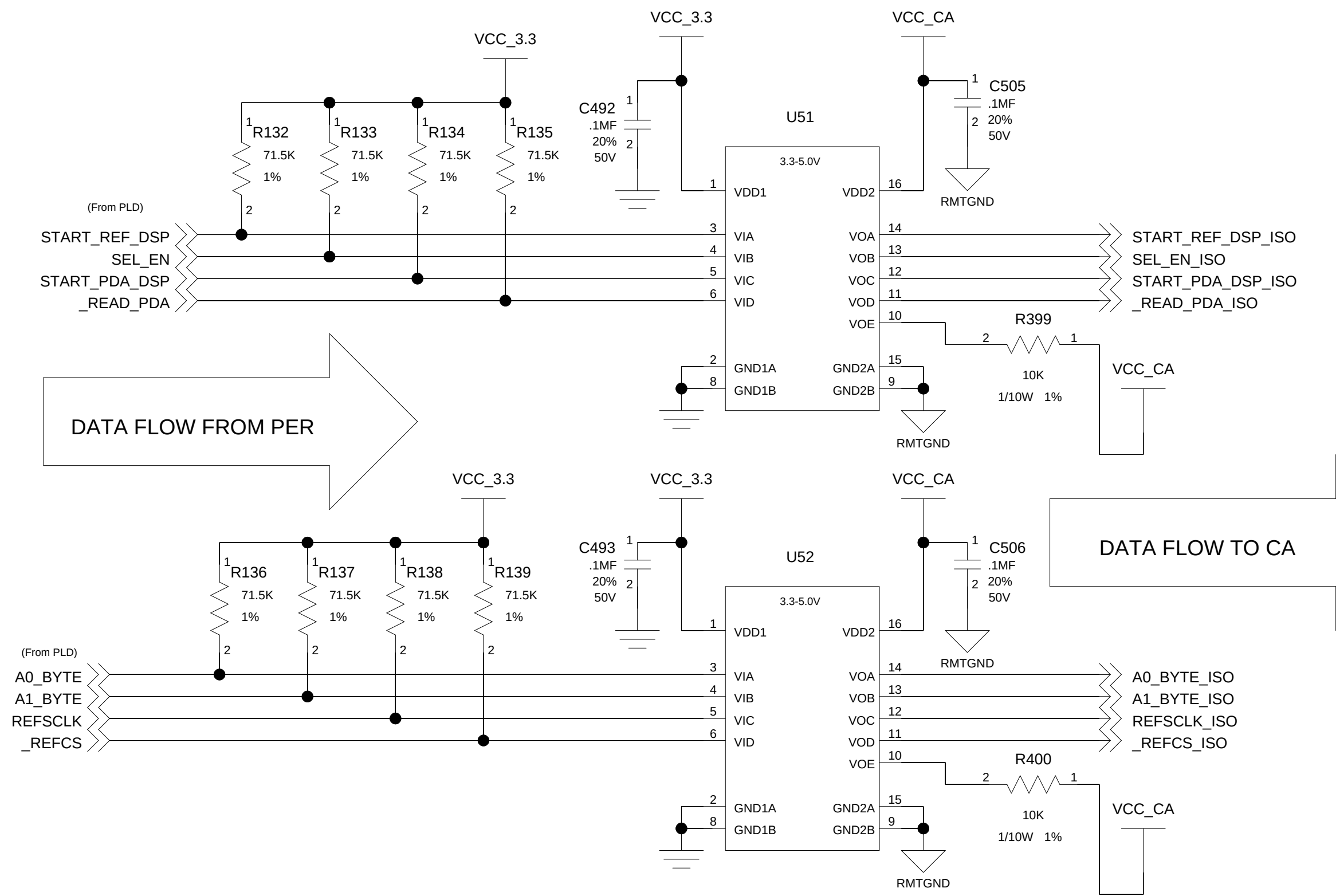


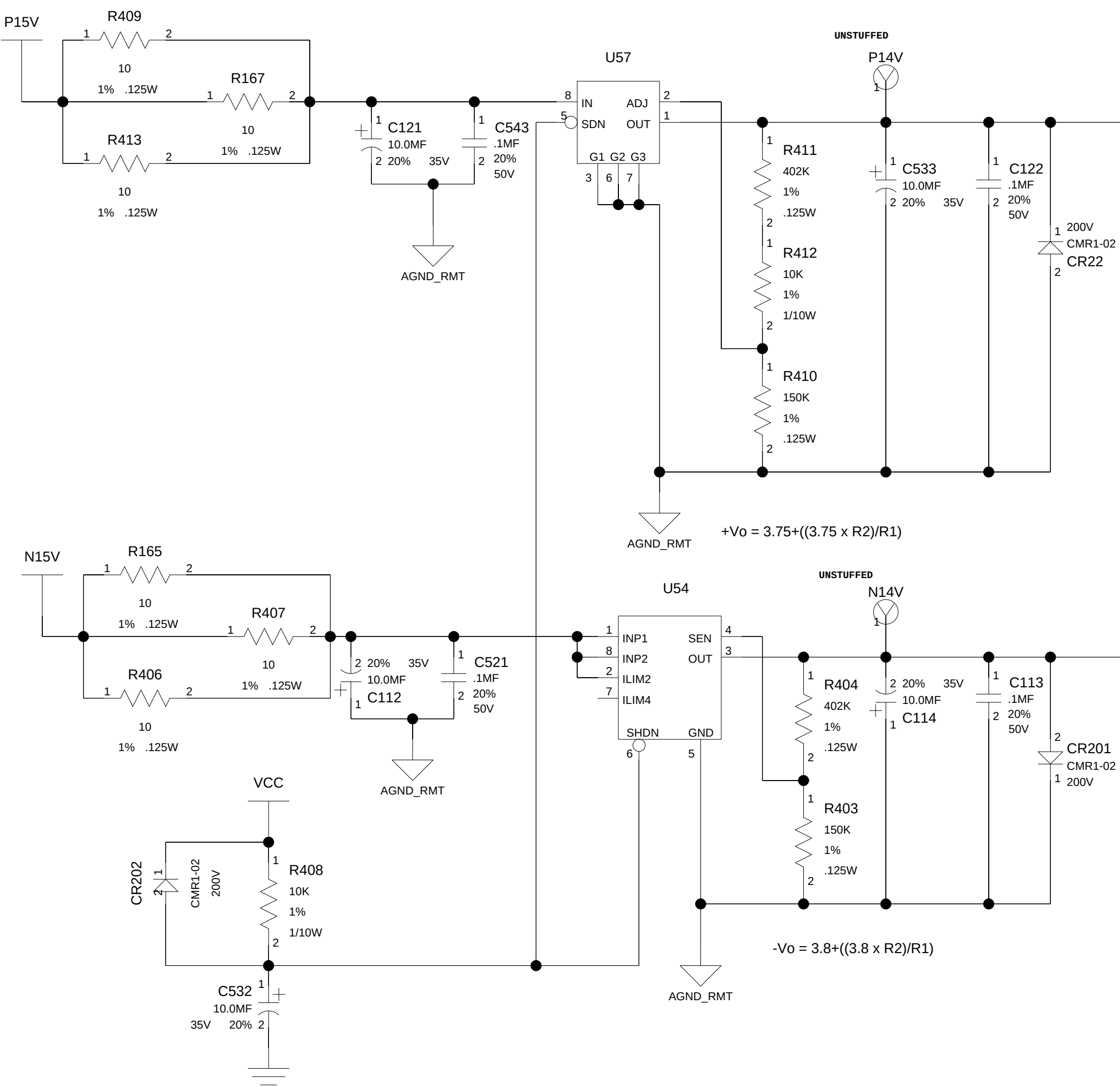
THIS DRAWING AND ALL INFORMATION HEREON IS THE PROPERTY OF WATERS CORP. ANY COPYING, REPRODUCTION OR UNAUTHORIZED USE IS FORBIDDEN WITHOUT WRITTEN CONSENT.

ISOLATED CONTROL SIGNALS FROM CA

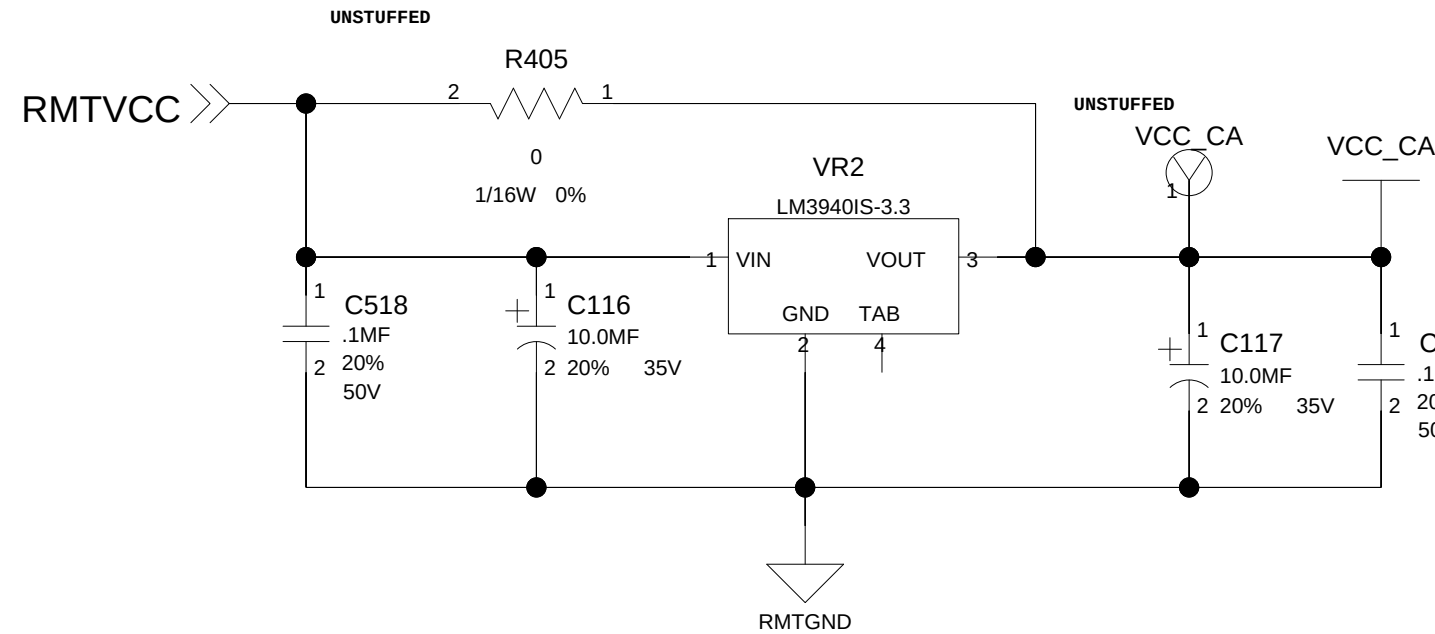


ISOLATED CONTROL SIGNALS FROM PER

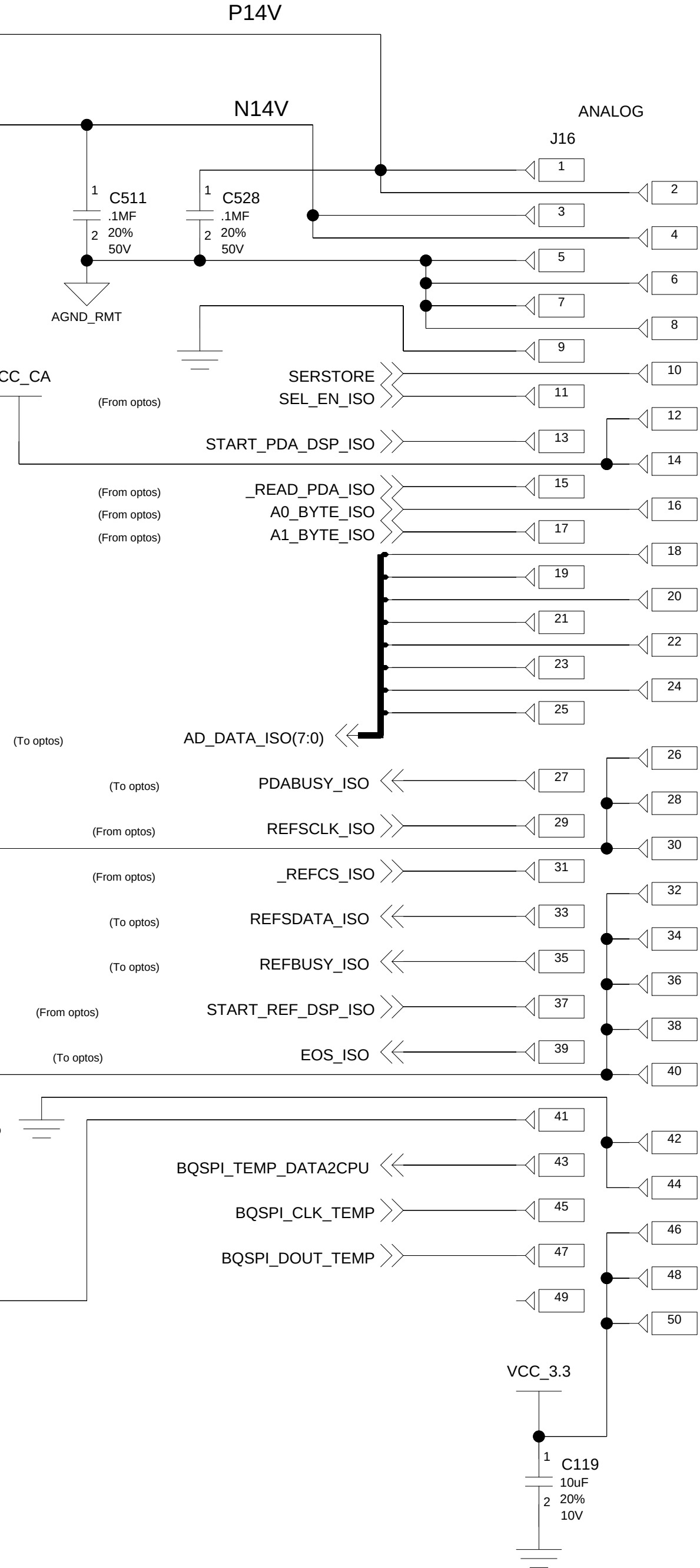
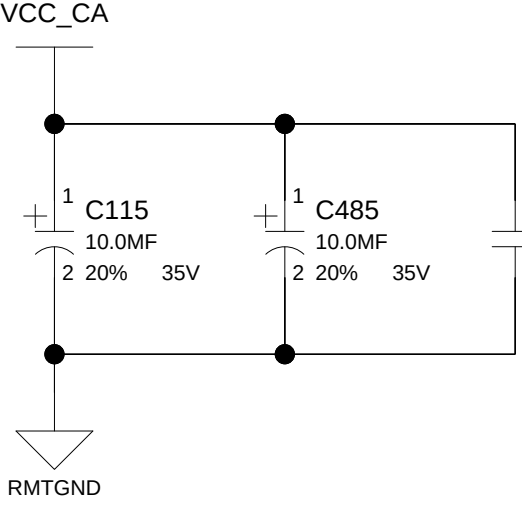




VCC_CA can be configured as 5v or 3.3v depending on BOM selection



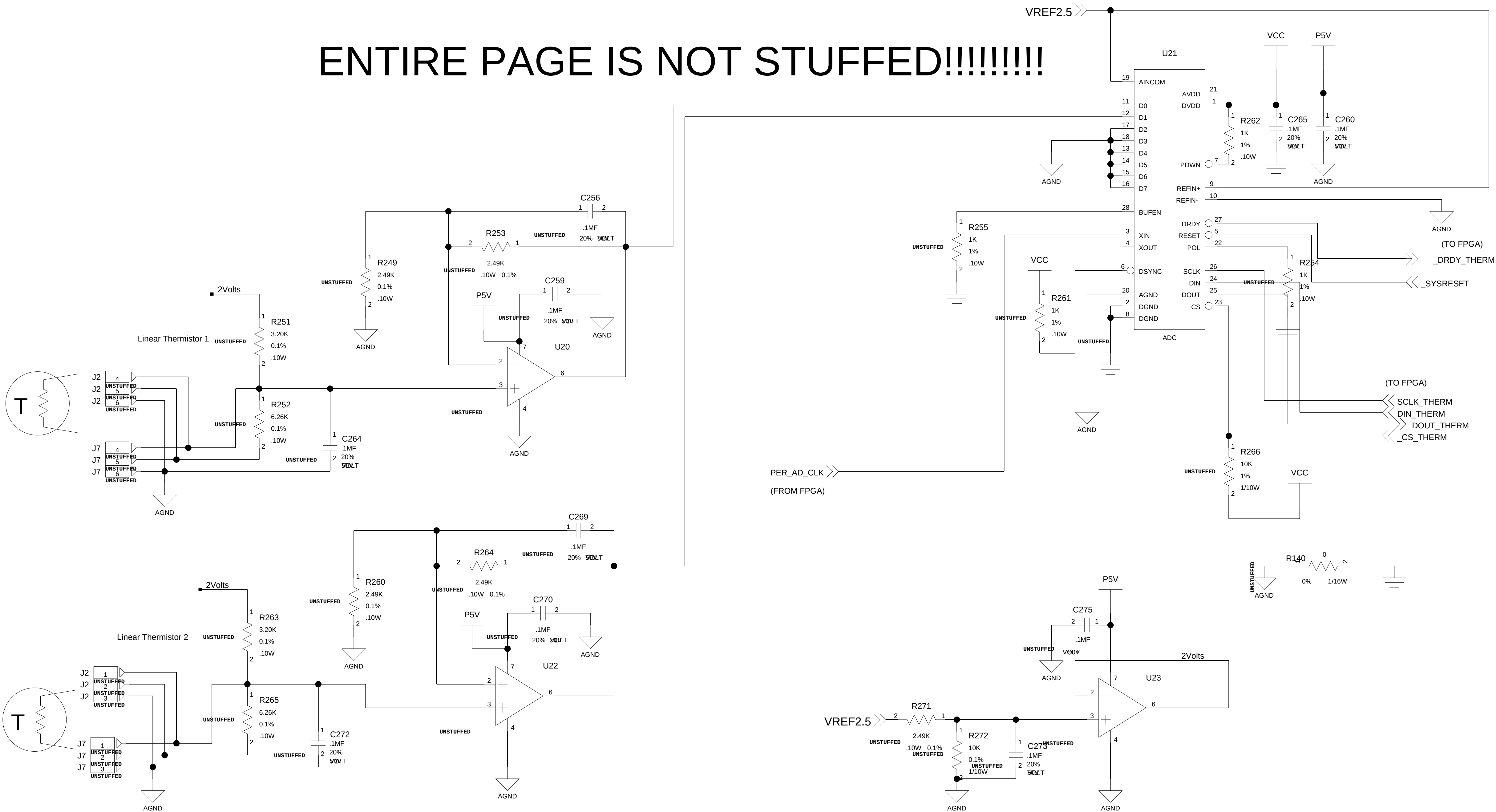
CHARGE AMP INTERFACE



CHARGE AMP BOARD

THERMISTOR CIRCUITS

ENTIRE PAGE IS NOT STUFFED!!!!!!!!!!

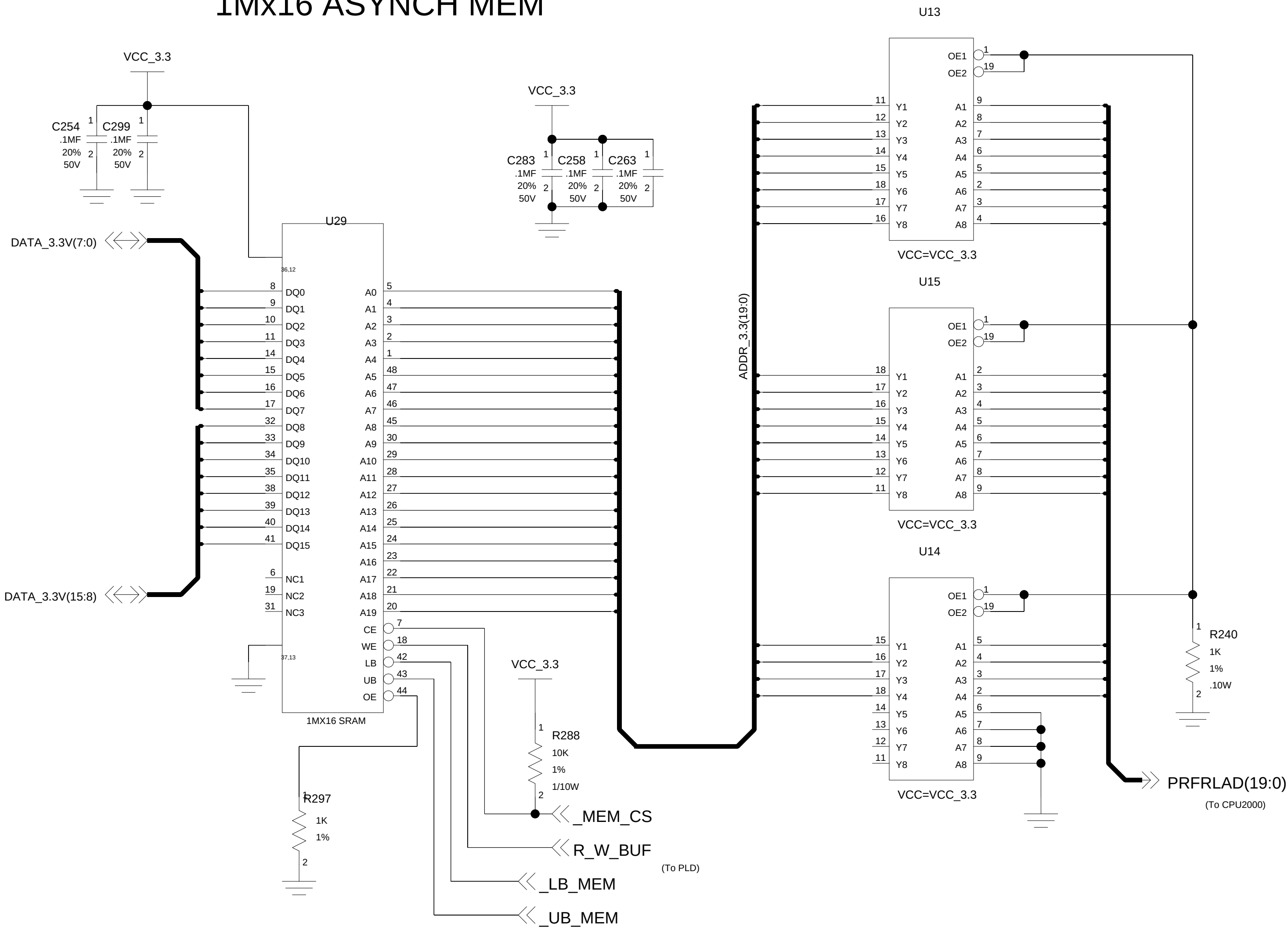


[illegible][illegible][illegible]

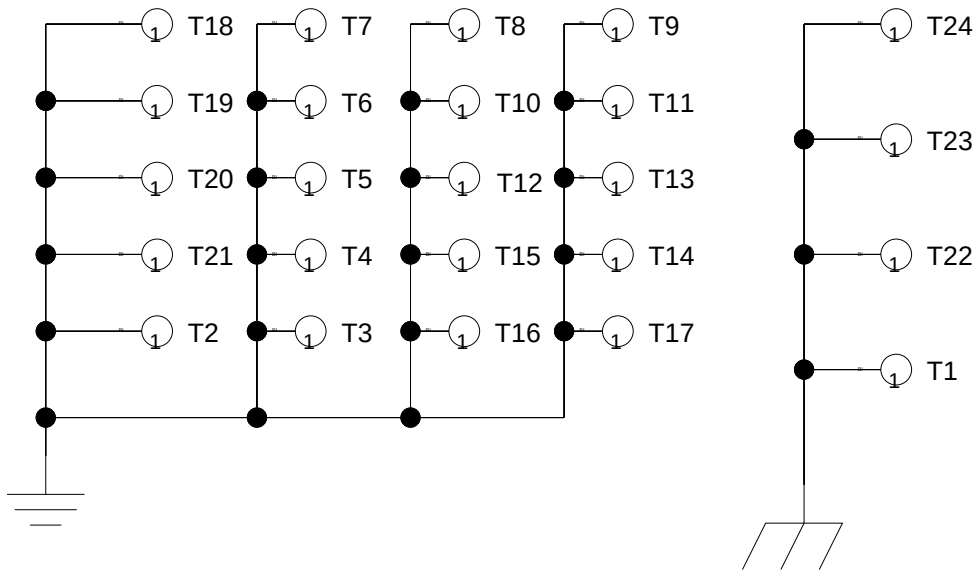
The schematic shows the 24V input and output connections for the AXC-TAN module. On the left, the 24V input is connected to a 24VDC source. The input is filtered by a 1M Ω , 20% tolerance capacitor (C488) connected to ground (24GND). The input signal is then split into three parallel paths, each passing through an unbuffered buffer (J17) before reaching the module's input pins (1, 2, and 3). On the right, the 50V output is connected to a 50VDC source. The output is filtered by a 1M Ω , 20% tolerance capacitor (C513) connected to ground (24GND). The output signal is then split into two parallel paths, each passing through an unbuffered buffer (J13) before reaching the module's output pins (1 and 2). The output signal is then connected to a load, represented by a circle with an 'X' inside.

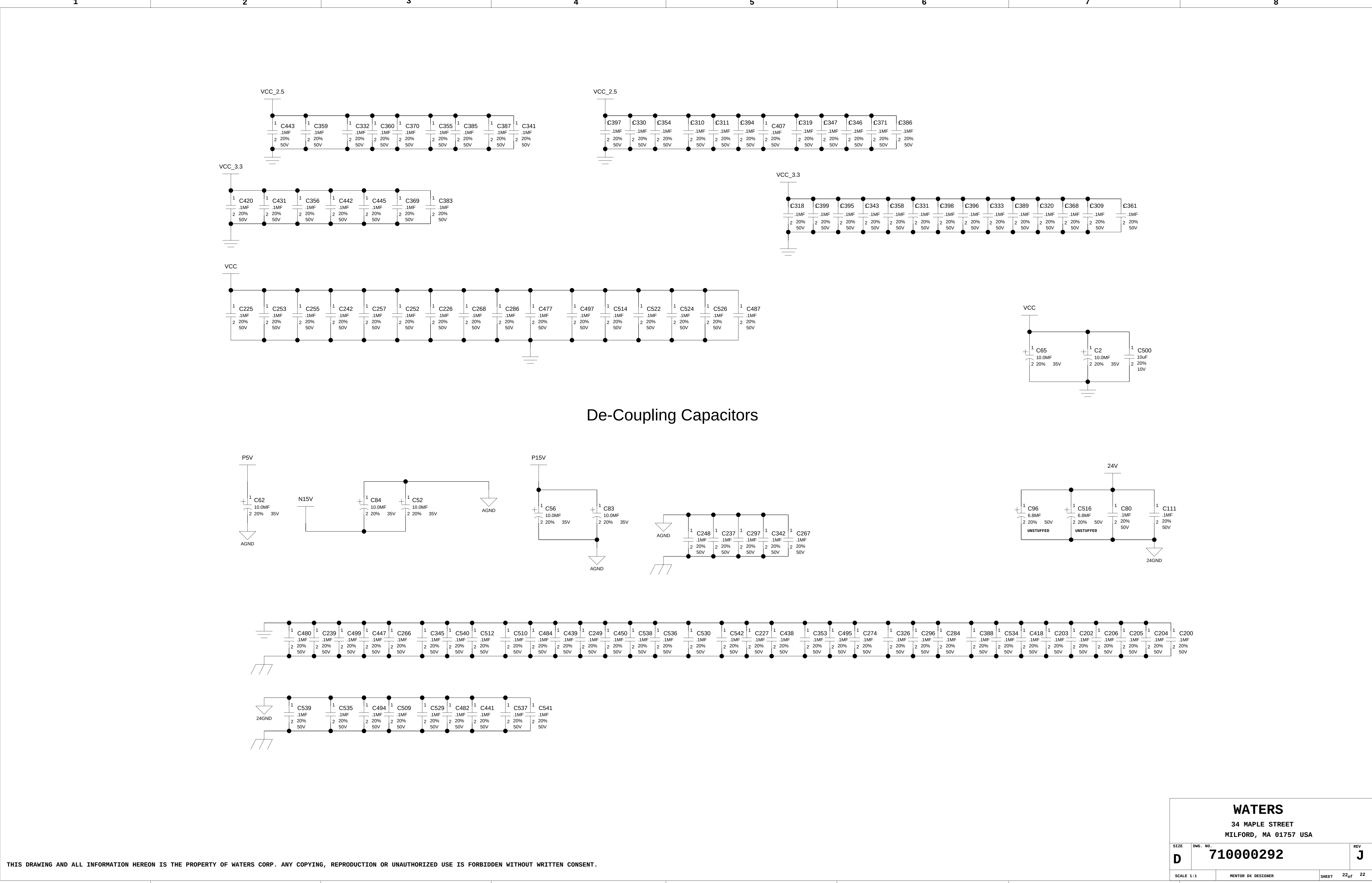
WATERS 34 MAPLE STREET MILFORD, MA 01757 USA			
SIZE D	DWG. NO. 710000292	REV J	
SCALE 1:1	MENTOR DX DESIGNER	SHEET	20 of 22

1Mx16 ASYNCH MEM



Memory is setup in this hardware config as 500Kx16.





THIS DRAWING AND ALL INFORMATION HEREON IS THE PROPERTY OF WATERS CORP. ANY COPYING, REPRODUCTION OR UNAUTHORIZED USE IS FORBIDDEN WITHOUT WRITTEN CONSENT.

WATERS			
34 MAPLE STREET			
MILFORD, MA 01757 USA			
SIZE	DWG. NO.	REV	
D	710000292	J	
SCALE 1:1		MENTOR DX DESIGNER	SHEET 22 of 22