

WATERS CORPORATION

ENGINEERING TEST SPECIFICATION AND PROCEDURE

COMPANY CONFIDENTIAL

SYSTEM/ASSEMBLY NAME: **2996 Main Board**

PART NUMBER AFFECTED: **210000238**

TEST EQUIPMENT NAME: **Racal Freedom System Functional Tester**

TEST EQUIPMENT NUMBER: **TE82751**

TEST EQUIPMENT LOCATION: **Sparton Electronics, FL**

DOCUMENT NUMBER: **735000823**

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EQUIPMENT REQUIRED

Quantity	Part No	Description
1	TE82751	2996 Main Bd. Functional Test Fixture
1	TE82743	Racal Freedom System Functional Tester

DISPOSABLES REQUIRED

Quantity	Part Number	Description
NA		

REFERENCE DOCUMENTATION

Number	Description
810000179	Performance Specification
210000179	Board Assembly Drawing
710000179	Board Schematic

I. Introduction to the 2996 Main bd. Functional Test

The 2996 Functional Test Fixture mounted to the Racal Freedom Functional Test System is designed to functionally test the Water's Corporation 2996 Main board.

The UUT should have had an in-circuit test performed prior to testing on this station. This will screen out most catastrophic board problems.

The system uses a vacuum fixture to pull the board down into a bed of nails for test access. Most, but not all, test points are accessed at the UUT's connectors.

The EEPROMS, DSP, and PLD's must be preprogrammed in order to perform this procedure.

II. Functional Test System Features

The fixture used on the Racal Freedom Tester has an ID system to identify the correct fixture in the test code.

III. Setup Requirements

Note:

- 1) The UUT is powered up with one short connecting J20_6 to J20_8. The short enables the Manufacture Test Mode of operation. This allows special test operations. The UUT reads the shorts upon power up.
- 2) A carriage return is sent to the UUT between (before or after) each test following Section 4.0 to clear the communications buffers.
- 3) Upon power up, the UUT may take up to 10 seconds to boot-up and allow RS232 communications.

1. DC Voltages & Currents

1.1. +5VDC VCC Voltage

5VDC is applied to J5 pins 4(+) and 5,6(-). The voltage is measured at those points to verify the proper voltage. Test Limits: Lo= 4.75VDC Hi= 5.25VDC

1.2. +12VDC Voltage

12VDC is applied to J5 pins 1(+) and 2(-). The voltage is measured at those points to verify the proper voltage. Test Limits: Lo= 11.0VDC Hi= 12.6VDC

1.3. -12VDC Voltage

12VDC is applied to J5 pins 2(+) and 3(-). The voltage is measured at those points to verify the proper voltage. Test Limits: Lo= -12.6VDC Hi= -11.0VDC

1.4. +24VDC Voltage

24VDC is applied to J5 pins 8,9(+) and 7(-). The voltage is measured at those points to verify the proper voltage. Test Limits: Lo= 23.5VDC Hi= 24.5VDC

1.5. +5VDC VCC Current

The current is measured via the HP power supply inquiry of the +5VDC power supplied as described above. Test Limits: Lo= 360mA Hi= 1440mA

1.6. +12VDC Current

The current is measured via the HP power supply inquiry of the +12VDC power supplied as described above. Test Limits: Lo= 6.0mA Hi= 500.0mA

1.7. -12VDC Current

The current is measured via the HP power supply inquiry of the -12DC power supplied as described above. Test Limits: Lo= 6.0mA Hi= 500.0mA

1.8. +24VDC Current

The current is measured via the HP power supply inquiry of the +24VDC power supplied as described above. Test Limits: Lo= -10.0mA Hi= 10.0mA

1.9. P5V Regulator Voltage

Regulator output VR2_VOUT (+) and J5_2(-) is probed and measured for the proper voltage. Test Limits: Lo= 4.75VDC Hi= 5.25VDC

1.10. N5V Regulator Voltage

Regulator output U12_3 (+) and J5_2(-) is probed and measured for the proper voltage. Test Limits: Lo= -5.25VDC Hi= -4.75VDC

1.11. P15V Regulator Voltage

Regulator output VR1_VOUT (+) and J5_7(-) is probed and measured for the proper voltage. Test Limits: Lo= 11.00VDC Hi= 12.60VDC

2. **Vent Fan (J12) ||| SKIP THIS TEST due to parts removed from board |||**

The voltage is measured at connector J12 pins 1 and 4. 0.0VDC is expected at those points. Test Limits: Lo= -0.30VDC Hi= 0.30VDC

3. **Charge Amp Outputs (J8)**

3.1. 5A Output J8_13

The 5A output voltage is measured at J8_13(+) and J8_1(-). Test Limits: Lo= 4.75VDC Hi= 5.25VDC

3.2. 5A Output J8_14

The 5A output voltage is measured at J8_14(+) and J8_1(-). Test Limits: Lo= 4.75VDC Hi= 5.25VDC

3.3. 12A Output J8_19

The 12A output voltage is measured at J8_19(+) and J8_1(-). Test Limits: Lo= 11.0VDC Hi= 13.0VDC

3.4. 12A Output J8_20

The 12A output voltage is measured at J8_20(+) and J8_1(-). Test Limits: Lo= 11.0VDC Hi= 13.0VDC

3.5. -12A Output J8_15

The -12A output voltage is measured at J8_15(+) and J8_1(-).

Test Limits: Lo= -13.0VDC Hi= -11.0VDC

3.6. -12A Output J8_16

The -12A output voltage is measured at J8_16(+) and J8_1(-).

Test Limits: Lo= -13.0VDC Hi= -11.0VDC

3.7. DRES_ISO output J8_6

The DRES_ISO output signal is measured at J8_6(+) and J8_7(-). A signal with a 10 uSEC positive pulse width is expected. Test Limits: Lo=7.5 uSEC Hi= 12.5 uSEC

3.8. LO_ISO output J8_4

The LO_ISO output signal is measured at J8_4(+) and J8_1(-). A signal with a 5.7 uSEC positive pulse width is expected. Test Limits: Lo=5.0 uSEC Hi= 7.0 uSEC

3.9. HI_ISO output J8_2

The HI_ISO output signal is measured at J8_2(+) and J8_1(-). A signal with a 5.7 uSEC positive pulse width is expected. Test Limits: Lo=5.0 uSEC Hi= 7.0 uSEC

3.10. QRES_ISO output J8_12

The QRES_ISO output signal is measured at J8_12(+) and J8_18(-). A signal with a 10 uSEC positive pulse width is expected. Test Limits: Lo=7.5 uSEC Hi= 12.5 uSEC

3.11. PHASE_ISO output J8_8

The PHASE_ISO output signal is measured at J8_8(+) and J8_7(-). A signal with a 5 uSEC positive pulse width is expected. Test Limits: Lo=4.0 uSEC Hi= 6.0 uSEC

3.12. START_ISO output J8_10

The START_ISO output signal is measured at J8_10(+) and J8_18(-). A signal with a 9 uSEC positive pulse width is expected. Test Limits: Lo=8.0 uSEC Hi= 12.0 uSEC

3.13. SH_ISO output J8_5

The SH_ISO output signal is measured at J8_5(+) and J8_17(-). A signal with a 7.25 uSEC positive pulse width is expected. Test Limits: Lo=6.0 uSEC Hi= 8.0 uSEC

3.14. _SH_ISO output J8_9

The _SH_ISO output signal is measured at J8_9(+) and J8_17(-). A signal with a 3 uSEC positive pulse width is expected. Test Limits: Lo=2.0 uSEC Hi= 4.0 uSEC

4. **Status LED and VCC Output (J4)**

4.1. VCC Output J4_1

The VCC output voltage is measured at J4_1(+) and J5_6(-).

Test Limits: Lo= 4.75VDC Hi= 5.25VDC

4.2. STATUS LED Output J4_3

The STATUS output signal is measured at J4_3(+) and J5_6(-). A 1.2 Hz square wave signal is expected. The High and Low vdc values are measured and averaged. $((5 + 0) / 2 = 2.5\text{vdc})$.

Test Limits: Lo= 2.00VDC Hi= 3.00VDC

5. Communications on RS232 Port (J7)

An **ID** command is sent to the UUT via the RS232 console port J7. The port is set default for 38400 baud, 1 stop, 8 bit, no parity, no flow control. A response from the UUT is expected to verify the microprocessor is up alive and talking.

6. Shutter Driver Output (J13)

6.1. SH_DN Output J13_1 OFF

The SH_DN output signal is measured at J13_1(+) and J13_2(-). The output should be OFF.

Test Limits: Lo= -0.1VDC Hi= 0.1VDC

6.2. SH_DN Output J13_1 ON

A **SH 1** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J13_1(+) and J13_2(-). A positive 12vdc pulse for approximately 2 seconds is expected.

Test Limits: Lo= 9.0VDC Hi= 16.0VDC

6.3. SH_UP Output J13_2 OFF

The SH_DN output signal is measured at J13_1(+) and J13_2(-). The output should be OFF.

Test Limits: Lo= -0.1VDC Hi= 0.1VDC

6.4. SH_UP Output J13_2 ON

A **SH 0** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J13_1(+) and J13_2(-). A negative 12vdc pulse for approximately 2 seconds is expected.

Test Limits: Lo= -16.0VDC Hi= -9.0VDC

7. Lamp Fan Output (J11) [[[SKIP THIS TEST due to parts removed from board]]]

7.1. LFAN Output J11_1 ON

A **FAN 0 0 99** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J11_1(+) and J11_2(-). Test Limits: Lo= 10.0VDC Hi= 16.0VDC

7.2. LFAN Output J11_1 OFF

A **FAN 0 0 0** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J11_1(+) and J11_2(-). Test Limits: Lo= -0.3VDC Hi= 0.3VDC

8. Event Outputs and Inputs (J9)

The two output SPST relays are measured by tying one leg to ground and the other to a 5-vdc pull-up. The relay operation can be verified by measuring on the pull-up side, a digital logic level (0v or 5v).

8.1. Event Output 1- Relay Open

A **PD 13 1 0** command is sent to the UUT. The output is measured at J9_17 and J9_18.
Test Results: Expected Digital High.

8.2. Event Output 1- Relay Closed

A **PD 13 1 1** command is sent to the UUT. The output is measured at J9_17 and J9_18.
Test Results: Expected Digital Low.

8.3. Event Output 2- Relay Open

A **PD 13 1 0** command is sent to the UUT. The output is measured at J9_23 and J9_24.
Test Results: Expected Digital High.

8.4. Event Output 2- Relay Closed

A **PD 13 1 2** command is sent to the UUT. The output is measured at J9_23 and J9_24.
Test Results: Expected Digital Low.

8.5. Event Input 1- Open

J9_13 to J9_14 is open and J15 to J16 is open. A **PD 12 1** command is sent to the UUT via the RS232 console port J7 to query the input.
Test Result: Expected to read “event inputs read 0 pass?” as a return message.

8.6. Event Input 1- Closed

A relay shorts J9_13 to J9_14, while J15 to J16 is open. A **PD 12 1** command is sent to the UUT via the RS232 console port J7 to query the input.
Test Result: Expected to read “event inputs read 2 pass?” as a return message.

8.7. Event Input 2- Open

J9_13 to J9_14 is open and J15 to J16 is open. A **PD 12 1** command is sent to the UUT via the RS232 console port J7 to query the input.
Test Result: Expected to read “event inputs read 0 pass?” as a return message.

8.8. Event Input 2- Closed

J9_13 to J9_14 is open, while a relay shorts J15 to J16. A **PD 12 1** command is sent to the UUT via the RS232 console port J7 to query the input.
Test Result: Expected to read “event inputs read 1 pass?” as a return message.

9. **GPIB Handshake (J3)**

A fixture jumper shorts J9_34, J9_33, J9_32, J9_31, J9_30. This sets the GPIB address to 1. An **ID** command is sent to the UUT via the IEEE port J3. A response is expected from that command via port J3, to verify an active and functional port. Test Results: The return string should read “DET996” along with some additional data.

10. **EEPROM Initialization (U10)**

The Serial EEPROM must be initialized. This clears the locations required for Final Instrument Testing. An **INITEE** command is sent to the UUT via the RS232 console port J7 to initialize the EEPROM.

An **ID** command is sent to the UUT via the RS232 console port J7 to read the EEPROM. The data returned is verified to match the following results.

Test Results:

Lambda	1:	180.0 nm
Lambda	512:	810.0 nm
Lamp time:		0.0 hours, starts 0, successes 0

11. Analog Outputs (J9)

The Analog output calculation is: $((\text{Analog Output Value} / 33425) * 10^8) = \text{programmed value}$
There is a 0.010vdc offset from the programmed value.

11.1. Analog Output 1 _ 0.01vdc

A **PD 14 1 2 0000** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J9_1(+) and J9_2(-). Test Limits: Lo= -0.030VDC Hi= 0.030VDC

11.2. Analog Output 1 _ 1.01vdc

A **PD 14 1 2 29320** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J9_1(+) and J9_2(-). Test Limits: Lo= 0.970VDC Hi= 1.030VDC

11.3. Analog Output 1 _ 2.00vdc

A **PD 14 1 2 58400** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J9_1(+) and J9_2(-). Test Limits: Lo= 1.970VDC Hi= 2.030VDC

11.4. Analog Output 2 _ 0.01vdc

A **PD 14 1 1 0000** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J9_4(+) and J9_3(-). Test Limits: Lo= -0.030VDC Hi= 0.030VDC

11.5. Analog Output 2 _ 1.01vdc

A **PD 14 1 1 29320** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J9_4(+) and J9_3(-). Test Limits: Lo= 0.970VDC Hi= 1.030VDC

11.6. Analog Output 2 _ 2.00vdc

A **PD 14 1 1 58400** command is sent to the UUT via the RS232 console port J7. The voltage is measured at connector J9_4(+) and J9_3(-). Test Limits: Lo= 1.970VDC Hi= 2.030VDC

12. Video Input (J14)

The voltage input calculation is: 12vdc = 65536 bits. Therefore there is 12/65535= 0.000183105 v/bit.

12.1. Video Input _ 12vdc

A power supply supplies 12.0 vdc to J14_1(+) and J14_2(-). A **PD 205 1 25 20 40** command is sent to the UUT via the RS232 console port J7 to read the input. The results are calculated into volts.

Test Limits: Lo= 11.88VDC Hi= 12.12VDC

12.2. Video Input _ 3vdc

A power supply supplies 3.0 vdc to J14_1(+) and J14_2(-). A **PD 205 1 25 20 40** command is sent to the UUT via the RS232 console port J7 to read the input. The results are calculated into volts.
Test Limits: Lo= 2.88VDC Hi= 3.12VDC

13. **ADC U30 Inputs** **[[[SKIP THIS TEST due to parts removed from board]]]**

The eight analog inputs are verified by sending a read command to the UUT. The results are returned in uVDC and converted to VDC.

13.1. Analog Input 1 (12A)

A **PD 21 1 0** command is sent to the UUT via the RS232 console port J7 to read the input.
The Analog input is at U30 pin 9. The input is voltage divided 10 to 1 at U30.
Test Limits: Lo= 1.10VDC Hi= 1.30VDC

13.2. Analog Input 2 (-12A)

A **PD 21 1 4** command is sent to the UUT via the RS232 console port J7 to read the input.
The Analog input is at U30 pin 10. The input is voltage divided 10 to 1 at U30.
Test Limits: Lo= 1.10VDC Hi= 1.30VDC

13.3. Analog Input 3 (24V)

A **PD 21 1 1** command is sent to the UUT via the RS232 console port J7 to read the input.
The Analog input is at U30 pin 11. The input is voltage divided 10 to 1 at U30.
Test Limits: Lo= 2.30VDC Hi= 2.50VDC

13.4. Analog Input 4 (ANAOUT1)

A **PD 14 1 2 29917** command is sent to set AnalogOut1 to 1.25vdc, then a **PD 21 1 5** command is sent to the UUT via the RS232 console port J7 to read the input.
The Analog input is at U30 pin 12. The input is voltage divided 10 to 1 at U30.
Test Limits: Lo= 0.70VDC Hi= 1.50VDC

13.5. Analog Input 5 (ANAOUT2)

A **PD 14 1 1 29917** command is sent to set AnalogOut2 to 1.25vdc, then a **PD 21 1 2** command is sent to the UUT via the RS232 console port J7 to read the input.
The Analog input is at U30 pin 13. The input is voltage divided 10 to 1 at U30.
Test Limits: Lo= 0.70VDC Hi= 1.50VDC

13.6. Analog Input 6 (THERM1-J16) **[[[SKIP THIS TEST due to parts removed from board]]]**

A 200K-ohm resistor is connected to J16 to simulate a thermister. A **PD 21 1 6** command is sent to the UUT via the RS232 console port J7 to read the input. The Analog input is at U30 pin 14.
Test Limits: Lo= 2.40VDC Hi= 2.70VDC

13.7. Analog Input 7 (THERM2-J15) **[[[SKIP THIS TEST due to parts removed from board]]]**

A 200K-ohm resistor is connected to J15 to simulate a thermister. A **PD 21 1 3** command is sent to the UUT via the RS232 console port J7 to read the input. The Analog input is at U30 pin 15.
Test Limits: Lo= 2.40VDC Hi= 2.70VDC

13.8. Analog Input 8 (AGND)

A **PD 21 1 7** command is sent to the UUT via the RS232 console port J7 to read the input. The Analog input is at U30 pin 16. Test Limits: Lo= -0.004VDC Hi= 0.004VDC

14. Lamp Board Interface (J1)

14.1. CLK200K output J1_6 [[[**SKIP THIS TEST due to new PLD change**]]]

The CLK200K output signal is measured at J1_6(+) and J5_6(-). A clock signal with a 2.5 uSEC positive pulse width is expected. Test Limits: Lo=2.0 uSEC Hi= 3.0 uSEC

14.2. LAMP_ENB_ISO Output J1_2 High

A **PD 220 1 1 1** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_2(+) and J1_7(-). Test Results: Digital High expected.

14.3. LAMP_ENB_ISO Output J1_2 Low

A **PD 220 1 1 0** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_2(+) and J1_7(-). Test Results: Digital Low expected.

14.4. ARC_ISO Output J1_3 High

A **PD 220 1 3 1** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_3(+) and J1_7(-). Test Results: Digital High expected.

14.5. ARC_ISO Output J1_3 Low

A **PD 220 1 3 0** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_3(+) and J1_7(-). Test Results: Digital Low expected.

14.6. FIL_ISO Output J1_4 High

A **PD 220 1 2 1** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_4(+) and J1_7(-). Test Results: Digital High expected.

14.7. FIL_ISO Output J1_4 Low

A **PD 220 1 2 0** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_4(+) and J1_7(-). Test Results: Digital Low expected.

14.8. FBCNT_ISO Output J1_1 Low

A **PD 220 1 5 1** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_1(+) and J1_7(-). Test Results: Digital Low expected.

14.9. FBCNT_ISO Output J1_1 High

A **PD 220 1 5 0** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_1(+) and J1_7(-). Test Results: Digital High expected.

14.10. LAMP_ZERO_ISO Output J1_5 Low

A **PD 220 1 4 1** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_5(+) and J1_7(-). Test Results: Digital Low expected.

14.11. LAMP_ZERO_ISO Output J1_5 High

A **PD 220 1 4 0** command is sent to the UUT via the RS232 console port J7. The digital output is measured at connector J1_5(+) and J1_7(-). Test Results: Digital High expected.

14.12. ISENSE_ISO Input J1_9 High

J1_9 to J1_8 is open. A **PD 220 1 0** command is sent to the UUT via the RS232 console port J7 to query the input. Test Result: Expected to read “TPU channel 0 set to 0” as a return message.

14.13. ISENSE_ISO Input J1_9 Low

A relay shorts J1_9 to J1_8. A **PD 220 1 0** command is sent to the UUT via the RS232 console port J7 to query the input. Test Result: Expected to read “TPU channel 0 set to 1” as a return message.

14.14. Lamp LED Output J4_2 Pulse

The Lamp output signal is measured at J4_2(+) and J5_6(-). A 1.5 Hz square wave signal is expected. The High and Low vdc values are measured and averaged. $((5 + 0) / 2 = 2.5\text{vdc})$.
Test Limits: Lo= 2.00VDC Hi= 3.00VDC