

 THE SCIENCE OF WHAT'S POSSIBLE.™		Equipment Design Verification Report	
Report No: TE0084031-EDVR		Iteration No: 00	SAP No: TE0084031QX

EQUIPMENT DESIGN VERIFICATION REPORT
 For the 2690 Alliance CPU Test Fixture (TE0084031)

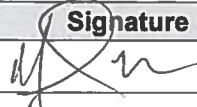
PREPARED BY

Name	Role	Signature	Date
Tyler Modelski	Test Engineer II		22 Jan 2019

REVIEWED BY

Name	Role	Signature	Date
Emma Pierce	Test Validation Engineer		22 Jan 2019

APPROVED BY

Name	Role	Signature	Date
Negan Marshall	Sr. Quality System Engineer		25 Jan 2019

The "Prepared By" signature denotes that this document accurately describes the verification activities.

The "Reviewed By" signature[s] denotes agreement with the description of the verification activities.

The "Approved By" signature denotes that this document has been reviewed and approved for overall quality and completeness.

REVISION HISTORY

Version	Author	Summary of change
00	Tyler Modelski	First document for approval

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1.0 Purpose

The 2690 Alliance CPU Functional Test Fixture facilitates the functional test for the 2690 Alliance CPU, Part #210000411. During the test, the UUT is connected and the test program on the GTS (TE82988) is launched. The automated test begins once the UUT serial number has been entered by the operator and the electrical performance of the test is verified. Tests include UUT startup, serial ports, onboard voltages, LED and beeper, serial options, diagnostics, CPU expansion bus, pressure acquisition, pump and fluidic drives, valve control, input changes, and relays. Upon completion, a Final Test Record is automatically generated and saved to the computer and a copy is sent to the CamStar7 Database. The operator can elect to print a hard copy of the report as well.

2.0 Scope of Report

This Equipment Design Verification Report details the verification activities undertaken for 2690 Alliance CPU Functional Test Fixture (TE0084031) based on the requirements of the executed protocol, TE0084031-EDV Iteration 01.

This EDV Report defines the documents used to verify the 2690 Alliance CPU Test Fixture Functional Test Fixture (TE0084031).

3.0 Summary of Results - Statement of Fitness for Intended Use

The 2690 Alliance CPU Functional Test Fixture (TE0084031) was tested in accordance with TE0084031-EDV Iteration 01. All test scripts were performed, all objective evidence requirements have been met, and all deviations resolved.

Waters now has the necessary documentation in place to ensure that the 2690 Alliance CPU Functional Test Fixture (TE0084031) complies with Waters' requirements, the latest relevant quality system regulations, and cGMP practices.

Following the approval of this EDV Report, the 2690 Alliance CPU Functional Test Fixture (TE0084031) can be considered fully verified and fit for intended use.

4.0 Glossary

The following definitions are used in this document:

Term	Explanation
>>>	Forward
<<<	Reverse
A	Amps
BAT	Batter
CLR	Clear
CPU	Central Processing Unit
EDV	Equipment Design Verification
EDVR	Equipment Design Verification Report
GND	Ground
GTS	Global Test System
ITA	Interface Test Adapter
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSL	Lower Specification Limit
MHz	Megahertz
ms	Milliseconds
MRR	Motor
NAN	Not a Number

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Term	Explanation
PSI	Pounds per Square Inch
PSI/V	Pounds Per Square Inch per Volts
PWR	Power
RAM	Random Access Memory
REF	Reference
ROM	Read Only Memory
TE	Test Engineering / Test Equipment
UI	User Interface
USL	Upper Specification Limit
UUT	Unit Under Test
V	Volts
VMP	Validation Master Plan
X, Y, Z	Three Dimensional Coordinate System

5.0 Training

The executor of the TE0084031-EDV Iteration 01 protocol was trained to the 730001835 procedure. Refer to Attachment #1 for a screenshot of the training database. The executor was also the author of the EDV protocol; therefore, no additional training was required.

6.0 Equipment Design Verification Results

The table below provides a summary of the results of the scripts executed as part of the TE0084031-EDV protocol. The objective evidence showing the results for each test step can be found in the attachments specified in the table.

Script or Section	Pass/Fail	Objective Evidence	Deviations
EDV-01	Pass	Attachments #2 and #3	#1
EDV-02	Pass	Attachments #4 and #5	#2, #3, #4, and #5

7.0 Attachments

Attachment #1: Training to 730001835 Process Validation Procedure Milford Site – Screenshot of Database

Attachment #2: Completed Test Script Data Sheet EDV-01: Specification and Functional Verification

Attachment #3: Test Record – Passing Result

Attachment #4: Completed Test Script Data Sheet EDV-02: Fault Insertion Test

Attachment #5: Screenshots of Test Software UI – Fault Insertion Testing

Attachment #6: Screenshot of Test Software Version

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8.0 Deviation from Equipment Design Verification

All deviations that occurred during execution of this EDV were protocol issues. None of the deviations affected the passing result of the EDV.

Deviation #1:

Description:

During the execution of script EDV-01, it was found that the LSL for Step 1.14 Measure_UUT_VddQuCurrent was incorrectly specified. The LSL should be 0.03A not 0.3A as indicated by the test report. This was an EDV protocol issue and the specification was corrected during the execution of the protocol.

Corrective Action:

To address this deviation the protocol has been updated to TE0084031-EDV Iteration 02 and changes to the Measure_UUT_VddQuCurrent acceptance criteria made as appropriate.

Conclusion:

The test successfully passed this test and was performed as intended. This deviation does not affect the result of this EDV report, and the overall result of the EDV remains a Pass.

Deviation #2:

Description:

During the execution of script EDV-02, it was found that the test step name for Step 12.4 was incorrect and should have been "LED DS4 Test". The correct test name can be found on the test report and in Step 12.4 of script EDV-01. This was an EDV protocol issue and the specification was corrected during the execution of the protocol.

Corrective Action:

To address this deviation the protocol has been updated to TE0084031-EDV Iteration 02 and changes to the LED DS4 Test name made as appropriate.

Conclusion:

The test successfully passed this test and was performed as intended. This deviation does not affect the result of this EDV report, and the overall result of the EDV remains a Pass.

Deviation #3:

Description:

During the execution of script EDV-02, it was found that there was no option for a "Pass" check box at the conclusion of the script. Both check boxes were labelled "Fail", and because the overall result of the script was a Pass, the addition of a pass label was necessary. This was an EDV protocol issue and the error was corrected during the execution of the protocol.

Corrective Action:

To address this deviation the protocol has been updated to TE0084031-EDV Iteration 02 and changes to the overall test conclusion of script EDV-02 made as appropriate.

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Conclusion:

The test successfully passed script EDV-02 and was performed as intended. This deviation does not affect the result of this EDV report, and the overall result of the EDV remains a Pass.

Deviation #4:

Description:

During the execution of script EDV-02, it was found that the expected result for Step 3.5 TestBat was incorrectly specified. The limit should be 2.9V not 2.96V as indicated by the test report. This was an EDV protocol issue and the specification was corrected during the execution of the protocol. The correct specification of 2.9V can be found in the test report as well as step 3.5 of script EDV-01.

Corrective Action:

To address this deviation the protocol has been updated to TE0084031-EDV Iteration 02 and changes to the Test Bat acceptance criteria made as appropriate.

Conclusion:

The test successfully passed this test and was performed as intended. This deviation does not affect the result of this EDV report, and the overall result of the EDV remains a Pass.

Deviation #5:

Description:

During the execution of script EDV-02, it was found that the units for Steps 1.4 Measure_UUT_VccQuCurrent and 1.13 Measure_UUT_VddQuCurrent were incorrect. The limit should be in amps (A) not volts (V) as indicated by the test report. This was an EDV protocol issue and the units were corrected during the execution of the protocol. The correct units can be found in the test report.

Corrective Action:

To address this deviation the protocol has been updated to TE0084031-EDV Iteration 02 and changes to the units made as appropriate.

Conclusion:

The test successfully passed this test and was performed as intended. This deviation does not affect the result of this EDV report, and the overall result of the EDV remains a Pass.

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9.0 References

The current approved versions of the following documents are referenced within this document:

Document Number	Document title
730001835	Process Validation Procedure for Milford Site
730002845	Validation Report Template
730001833	Test Engineering Management Policy
810000444	Perf Spec, PCB, EALLIANCE CPU ROHS
710000444	Schem, PCB, EALLIANCE CPU ROHS
TE0084031EQ	Test Equipment Design Documents, 2690 Alliance CPU Test Fixture
TE0084031QA	Equipment Design Verification Protocol, 2690 Alliance CPU Test Fixture
735002109	TSP, Waters GTS Operation
735004006	Waters GTS Preventative Maintenance and Cal



Waters

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CERTIFICATE OF COMPLETION

This certificate is presented to

Tyler Modelski

for successfully completing

Process Validation Procedure for Milford (Ver 07)

Training

16 October 2018

Issue Date

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Attachment: #1 Page: 1 of 1

This certificate is only valid while the above named representative is employed by or an authorized agent of Waters Corporation, and performance can be monitored, updated and certification guaranteed.

Report No: TE0084031-EDV

Iteration No: 01

SAP No: TE0084031QA

Test name: Specification and Functional Verification

Test Script No.: EDV-01

Equipment Number: TE0084031

Equipment Name: 2690 Alliance CPU Assembly Test Fixture

Software Version: 0.0

Part Number: 210000411

Serial Number: 160618132M

Purpose:

To ensure that obtained results that are within specification are measured/reported as such by the system.
To ensure that critical to quality specifications are properly implemented for test.

Test execution:

Perform the Test Script steps in order to verify system specifications and functionality.

Run the equipment until completion. Verify that all acceptance criteria listed below are met and documented on the Final Test Record.

Objective evidence:

Completed Test Script Data Sheet

Copy of the Final Test record(s) for each UUT

Description Specification	Acceptance Criteria	Actual Result	Pass / Fail	Initial & Date
1. UUT Startup	PASS	Pass	Pass	TJM 14 Jan 2019
1.1. CPU Reset Duration	LSL = 3.30 ms USL = 4.00 ms	3.55 ms	Pass	TJM 14 Jan 2019
1.2. ExtSysResetDuration	LSL = 0.30 ms USL = 0.70 ms	0.33 ms	Pass	TJM 14 Jan 2019
1.3. PowerVcc_SupplyStatus	Pass	Pass	Pass	TJM 14 Jan 2019
1.4. Measure_UUT_VccQuCurrent	LSL = 0.30 A USL = 0.80 A	0.576 A	Pass	TJM 14 Jan 2019
1.5. Startup	Pass	Pass	Pass	TJM 14 Jan 2019
1.6. TE Firmware Installed	Pass	Pass	Pass	TJM 14 Jan 2019
1.7. SerialOptScanning	Pass	Pass	Pass	TJM 14 Jan 2019
1.8. SerialOptStartupSlot:0	Pass	Pass	Pass	TJM 14 Jan 2019
1.9. SerialOptStartupSlot:1	Pass	Pass	Pass	TJM 14 Jan 2019
1.10. SerialOptStartupSlot:2	Pass	Pass	Pass	TJM 14 Jan 2019
1.11. SerialOptStartupSlot:3	Pass	Pass	Pass	TJM 14 Jan 2019
1.12. CheckDiags	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.1. CheckDiag:CPUTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.2. CheckDiag:ROMTest	Pass	Pass	Pass	TJM 14 Jan 2019

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1.12.3. CheckDiag:RAMTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.4. CheckDiag:BeeperPresentTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.5. CheckDiag:LedPresentTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.6. CheckDiag:KeypadPresentTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.7. CheckDiag:DisplayPresentTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.8. CheckDiag:DMATest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.9. CheckDiag:GpibTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.10. CheckDiag:FlashTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.11. CheckDiag:DSPTTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.12. CheckDiag:FloppyTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.13. CheckDiag:ClockTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.14. CheckDiag:ClockRunningTest	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.15. CheckDiag:BatteryCheck	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.16. Check CPU Real Time Clock	Pass	Pass	Pass	TJM 14 Jan 2019
1.12.17. Set Date	Pass	Pass	Pass	TJM 14 Jan 2019
1.13. PowerVdd_SupplyStatus	Pass	Pass	Pass	TJM 14 Jan 2019
1.14. Measure_UUT_VddQuCurrent	LSL = 0.03 A USL = 0.10 A <i>see derivation #1 TJM 25 Jan 2019 0.069 A</i>	Pass	Pass	TJM 14 Jan 2019
1.15. DiagComTest	Pass	Pass	Pass	TJM 14 Jan 2019
2. TestSerialOptions	PASS	Pass	Pass	TJM 14 Jan 2019
2.1. SerialOptionCPUWrt	Pass	Pass	Pass	TJM 14 Jan 2019
2.2. SerialOptCPUWrtSlot: 0	Pass	Pass	Pass	TJM 14 Jan 2019
2.3. SerialOptCPUWrtSlot: 1	Pass	Pass	Pass	TJM 14 Jan 2019
2.4. SerialOptCPUWrtSlot: 2	Pass	Pass	Pass	TJM 14 Jan 2019
2.5. SerialOptCPUWrtSlot: 3	Pass	Pass	Pass	TJM 14 Jan 2019
2.6. SerialOptionRead	Pass	Pass	Pass	TJM 14 Jan 2019
2.7. SerialOptCPUReadCmdSlot: 0	Pass	Pass	Pass	TJM 14 Jan 2019
2.8. SerialOptCPUReadCmdSlot: 1	Pass	Pass	Pass	TJM 14 Jan 2019

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2.9. SerialOptCPUReadCmdSlot: 2	Pass	Pass	Pass	TJM 14Jan2019
2.10. SerialOptCPUReadCmdSlot: 3	Pass	Pass	Pass	TJM 14Jan2019
2.11. SerialOptCPUReadMOSI_Slot: 0	Pass	Pass	Pass	TJM 14Jan2019
2.12. SerialOptCPUReadMOSI_Slot: 1	Pass	Pass	Pass	TJM 14Jan2019
2.13. SerialOptCPUReadMOSI_Slot: 2	Pass	Pass	Pass	TJM 14Jan2019
2.14. SerialOptCPUReadMOSI_Slot: 3	Pass	Pass	Pass	TJM 14Jan2019
3. TestOnboardVoltages	PASS	Pass	Pass	TJM 14Jan2019
3.1. Test 5VRef	LSL = 4.90 V USL = 5.10 V	5.011 V	Pass	TJM 14Jan2019
3.2. Test 3.3VPwr	LSL = 3.20 V USL = 3.50 V	3.342 V	Pass	TJM 14Jan2019
3.3. Test 2.5VPwr	LSL = 2.40 V USL = 2.70 V	2.515 V	Pass	TJM 14Jan2019
3.4. Test 1.8VPwr	LSL = 1.75 V USL = 1.85 V	1.805 V	Pass	TJM 14Jan2019
3.5. TestBat	LSL = 2.90 V USL = 3.50 V	3.084 V	Pass	TJM 14Jan2019
3.6. TestAnalogOut	LSL = -0.10 V USL = 0.10 V	0.01 V	Pass	TJM 14Jan2019
4. TestCPUExpBus	PASS	Pass	Pass	TJM 14Jan2019
4.1. TestFrontPanelReadVideoData	Pass	Pass	Pass	TJM 14Jan2019
4.2. TestFrontPanelWriteVideoData	Pass	Pass	Pass	TJM 14Jan2019
4.3. TestFrontPanelReadKeyData	Pass	Pass	Pass	TJM 14Jan2019
4.4. TestFrontPanelWriteBackLightData	Pass	Pass	Pass	TJM 14Jan2019
4.5. TestFrontPanelWriteLCDPage	Pass	Pass	Pass	TJM 14Jan2019
4.6. TestFrontPanelReadIntpReg	Pass	Pass	Pass	TJM 14Jan2019
4.7. TestFrontPanelIntp	Pass	Pass	Pass	TJM 14Jan2019
4.8. TestFluidicsReadSensorReg1	Pass	Pass	Pass	TJM 14Jan2019
4.9. TestFluidicsReadSensorReg2	Pass	Pass	Pass	TJM 14Jan2019
4.10. TestFluidicsWriteMotorEnableReg	Pass	Pass	Pass	TJM 14Jan2019

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4.11. TestFluidicsWriteMotorHoldReg	Pass	Pass	Pass	TJM 14Jan2019
4.12. TestFluidicsWriteMotorControlReg	Pass	Pass	Pass	TJM 14Jan2019
5. TestPressAcqu	PASS	Pass	Pass	TJM 14Jan2019
5.1. CheckPrimary Offset	LSL = 0.00 psi USL = 60.00 psi	41.22 psi	Pass	TJM 14Jan2019
5.2. CheckPrimary psi/V	LSL = 2150.00 psi/V USL = 2250.00 psi/V	2192.64 psi/V	Pass	TJM 14Jan2019
5.3. TestPrimaryMidPressure	LSL = -10.00 psi USL = 10.00 psi	-0.47 psi	Pass	TJM 14Jan2019
5.4. TestPrimaryHighPressure	LSL = -10.00 psi USL = 10.00 psi	-0.67 psi	Pass	TJM 14Jan2019
5.5. CheckSystem Offset	LSL = 0.00 psi USL = 60.00 psi	41.9 psi	Pass	TJM 14Jan2019
5.6. CheckSystem psi/V	LSL = 2150.00 psi/V USL = 2250.00 psi/V	2193.05 psi/V	Pass	TJM 14Jan2019
5.7. TestSystemMidPressure	LSL = -10.00 psi USL = 10.00 psi	-0.33 psi	Pass	TJM 14Jan2019
5.8. TestSystemHighPressure	LSL = -10.00 psi USL = 10.00 psi	-0.93 psi	Pass	TJM 14Jan2019
5.9. CheckSample Offset	LSL = 0.00 psi USL = 60.00 psi	37.06 psi	Pass	TJM 14Jan2019
5.10. CheckSample psi/V	LSL = 2150.00 psi/V USL = 2250.00 psi/V	2193.06 psi/V	Pass	TJM 14Jan2019
5.11. TestSampleMidPressure	LSL = -10.00 psi USL = 10.00 psi	-0.47 psi	Pass	TJM 14Jan2019
5.12. TestSampleHighPressure	LSL = -10.00 psi USL = 10.00 psi	-0.80 psi	Pass	TJM 14Jan2019
5.13. VerifyOvrPressEventsClr	Pass	Pass	Pass	TJM 14Jan2019
5.14. CheckPrimOvrPressEvent	Pass	Pass	Pass	TJM 14Jan2019
5.15. VerifyPrmOvrPressEventsClr	Pass	Pass	Pass	TJM 14Jan2019
5.16. CheckAccumOvrPressEvent	Pass	Pass	Pass	TJM 14Jan2019
5.17. VerifyAccumOvrPressEventsClr	Pass	Pass	Pass	TJM 14Jan2019

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6. TestPumpDrive	PASS	Pass	Pass	TJM 14Jan2019
6.1. VerifyPumpEventsClr	Pass	Pass	Pass	TJM 14Jan2019
6.2. MotorPowerEnabled	Pass	Pass	Pass	TJM 14Jan2019
6.3. TestPrimaryPump	Pass	Pass	Pass	TJM 14Jan2019
6.4. TestAccumPump	Pass	Pass	Pass	TJM 14Jan2019
6.5. Test GPV Fail	Pass	Pass	Pass	TJM 14Jan2019
6.6. Test MTR Fail	Pass	Pass	Pass	TJM 14Jan2019
6.7. Motor Power Disabled	Pass	Pass	Pass	TJM 14Jan2019
7. TestValveControl	PASS	Pass	Pass	TJM 14Jan2019
7.1. TestGPVControl_NONE	Pass	Pass	Pass	TJM 14Jan2019
7.2. TestGPVControl_A	Pass	Pass	Pass	TJM 14Jan2019
7.3. TestGPVControl_B	Pass	Pass	Pass	TJM 14Jan2019
7.4. TestGPVControl_C	Pass	Pass	Pass	TJM 14Jan2019
7.5. TestGPVControl_D	Pass	Pass	Pass	TJM 14Jan2019
7.6. TestSealWashOff	Pass	Pass	Pass	TJM 14Jan2019
7.7. TestSealWashOn	Pass	Pass	Pass	TJM 14Jan2019
7.8. TestSpurgeAOff	Pass	Pass	Pass	TJM 14Jan2019
7.9. TestSpurgeAOn	Pass	Pass	Pass	TJM 14Jan2019
7.10. TestSpurgeBOff	Pass	Pass	Pass	TJM 14Jan2019
7.11. TestSpurgeBOn	Pass	Pass	Pass	TJM 14Jan2019
7.12. TestSpurgeCOff	Pass	Pass	Pass	TJM 14Jan2019
7.13. TestSpurgeCOn	Pass	Pass	Pass	TJM 14Jan2019
7.14. TestSpurgeDOff	Pass	Pass	Pass	TJM 14Jan2019
7.15. TestSpurgeDOn	Pass	Pass	Pass	TJM 14Jan2019
8. TestEventsOut	PASS	Pass	Pass	TJM 14Jan2019
8.1. TestEventsOut_Set0	Pass	Pass	Pass	TJM 14Jan2019
8.2. TestEventsOut_Clr0	Pass	Pass	Pass	TJM 14Jan2019

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8.3. TestEventsOut_Set1	Pass	Pass	Pass	TJM 14 Jan 2019
8.4. TestEventsOut_Clr1	Pass	Pass	Pass	TJM 14 Jan 2019
8.5. TestEventsOut_Set2	Pass	Pass	Pass	TJM 14 Jan 2019
8.6. TestEventsOut_Clr2	Pass	Pass	Pass	TJM 14 Jan 2019
8.7. TestEventsOut_Set3	Pass	Pass	Pass	TJM 14 Jan 2019
8.8. TestEventsOut_Clr3	Pass	Pass	Pass	TJM 14 Jan 2019
8.9. TestEventsOut_Set4	Pass	Pass	Pass	TJM 14 Jan 2019
8.10. TestEventsOut_Clr4	Pass	Pass	Pass	TJM 14 Jan 2019
8.11. TestEventsOut_Set5	Pass	Pass	Pass	TJM 14 Jan 2019
8.12. TestEventsOut_Clr5	Pass	Pass	Pass	TJM 14 Jan 2019
9. TestFluidicDrive	PASS	Pass	Pass	TJM 14 Jan 2019
9.1. V1Motor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.2. V1Motor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.3. V2Motor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.4. V2Motor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.5. ZCarouselMotor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.6. ZCarouselMotor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.7. DisMotor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.8. DisMotor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.9. SyringeMotor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.10. SyringeMotor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.11. NeedleMotor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.12. NeedleMotor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.13. XMotor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.14. XMotor<<<	Pass	Pass	Pass	TJM 14 Jan 2019
9.15. YMotor>>>	Pass	Pass	Pass	TJM 14 Jan 2019
9.16. YMotor<<<	Pass	Pass	Pass	TJM 14 Jan 2019

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9.17. ZMotor>>>	Pass	Pass	Pass	TJM 14Jan2019
9.18. ZMotor<<<	Pass	Pass	Pass	TJM 14Jan2019
9.19. RocketMotor>>>	Pass	Pass	Pass	TJM 14Jan2019
9.20. RocketMotor<<<	Pass	Pass	Pass	TJM 14Jan2019
9.21. CarrierMotor>>>	Pass	Pass	Pass	TJM 14Jan2019
9.22. CarouselMotor>>>	Pass	Pass	Pass	TJM 14Jan2019
9.23. MeasFluidicClock	LSL = 9.99 MHz USL = 10.10 MHz	10 MHz	Pass	TJM 14Jan2019
10. TestPorts	PASS	Pass	Pass	TJM 14Jan2019
10.1. TestRemotePort	Pass	Pass	Pass	TJM 14Jan2019
10.2. Ethernet Test	Pass	Pass	Pass	TJM 14Jan2019
10.3. GPIBUUT_SlaveReceive	Pass	Pass	Pass	TJM 14Jan2019
10.4. GPIBUUT_SlaveReply	Pass	Pass	Pass	TJM 14Jan2019
10.5. TestFloppyControl	Pass	Pass	Pass	TJM 14Jan2019
11. TestEventsIn	PASS	Pass	Pass	TJM 14Jan2019
11.1. ActiveLow_0	Pass	Pass	Pass	TJM 14Jan2019
11.2. ActiveLow_1	Pass	Pass	Pass	TJM 14Jan2019
11.3. ActiveLow_2	Pass	Pass	Pass	TJM 14Jan2019
11.4. ActiveHigh_0	Pass	Pass	Pass	TJM 14Jan2019
11.5. ActiveHigh_1	Pass	Pass	Pass	TJM 14Jan2019
11.6. ActiveHigh_2	Pass	Pass	Pass	TJM 14Jan2019
12. BeepLedReset	PASS	Pass	Pass	TJM 14Jan2019
12.1. LED DS1 Test	Pass	Pass	Pass	TJM 14Jan2019
12.2. LED DS2 Test	Pass	Pass	Pass	TJM 14Jan2019
12.3. LED DS3 Test	Pass	Pass	Pass	TJM 14Jan2019
12.4. LED DS4 Test	Pass	Pass	Pass	TJM 14Jan2019
12.5. LED DS5 Test	Pass	Pass	Pass	TJM 14Jan2019
12.6. LED DS6 Test	Pass	Pass	Pass	TJM 14Jan2019

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12.7. LED DS7 Test	Pass	Pass	Pass	TJM 14Jun2019
12.8. LED DS8 Test	Pass	Pass	Pass	TJM 14Jun2019
12.9. Beeper Test	Pass	Pass	Pass	TJM 14Jun2019

Comments:

There is an EDV protocol issue in step 1.14. The LSL should be 0.03A, not 0.3A, as found on the test report. Refer to deviation #1. TJM 14Jan2019

Overall Test Conclusion:☒ Pass☐ Fail

 Expand/Collapse All Loop Indices

UUT Report

- Station ID: TE82988-1
- Serial Number: 160618132M
- Date: Monday, January 14, 2019
- Time: 9:36:30 AM
- Operator: administrator
- Execution Time: 341.504964 seconds
- Number of Results: 212
- UUT Result: Passed

Begin Sequence: MainSequence
(C:\GTS Files\Sequences\210000411\210000411.seq)

ValidSerialNumber	
Status:	Passed
Software Revision	
Status:	Done
Software Revision:	TE0084031SF VER:0.0
UUTStartup	
Status:	Passed
Module Time:	67.0613573

Begin Sequence: UUTStartup
(C:\GTS Files\Sequences\210000411\210000411.seq)

Init Mux	
Status:	Running
Number of Loops:	1
 Init Mux (Loop Indices)	

CPU Reset Duration	
Status:	Passed
Numeric:	3.55
Units:	ms
Limits:	
Low:	3.30
High:	4.00
Comp:	GELE
ExtSySResetDuration	
Status:	Passed
Numeric:	0.33
Units:	ms
Limits:	
Low:	0.30
High:	0.70

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Comp:	GELE
PowerVcc_SupplyStatus	
Status:	Passed
Module Time:	0.054552
Measure_UUT_VccQuCurrent	
Status:	Passed
Numeric:	0.576
Units:	A
Limits:	
Low:	0.3
High:	0.8
Comp:	GELE
Module Time:	0.6269668
Serial Option Discovery	
Status:	Done
Startup	
Status:	Passed
Module Time:	42.6958993
Installed Firmware:Alliance 2690 Boot Strap LoaderAug 5 2008 at 18:12:02	
TE Firmware Installed	
Status:	Passed
SerialOptScanning	
Status:	Passed
SerialOptStartupSlot:0	
Status:	Passed
SerialOptStartupSlot:1	
Status:	Passed
SerialOptStartupSlot:2	
Status:	Passed
SerialOptStartupSlot:3	
Status:	Passed
CheckDiags	
Status:	Passed
Module Time:	6.8065505

Begin Sequence: CheckDiags
(C:\GTS Files\Sequences\210000411\210000411.seq)

Check Startup Diags	
Status:	Done
CheckDiag:CPUTest	
Status:	Passed
Module Time:	0.0022653
CheckDiag:ROMTest	
Status:	Passed
Module Time:	0.0019562
CheckDiag:RAMTest	
Status:	Passed

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Module Time:	0.0018117
CheckDiag:BeeperPresentTest	
Status:	Passed
Module Time:	0.001823
CheckDiag:LedPresentTest	
Status:	Passed
Module Time:	0.0017864
CheckDiag:KeypadPresentTest	
Status:	Passed
Module Time:	0.0018775
CheckDiag:DisplayPresentTest	
Status:	Passed
Module Time:	0.0018392
CheckDiag:DMATest	
Status:	Passed
Module Time:	0.0021749
CheckDiag:GpibTest	
Status:	Passed
Module Time:	0.0022115
CheckDiag:FlashTest	
Status:	Passed
Module Time:	0.0021866
CheckDiag:DSPTest	
Status:	Passed
Module Time:	0.0019188
CheckDiag:FloppyTest	
Status:	Passed
Module Time:	0.001972
CheckDiag:ClockTest	
Status:	Passed
Module Time:	0.0018718
CheckDiag:ClockRunningTest	
Status:	Passed
Module Time:	0.0018196
CheckDiag:BatteryCheck	
Status:	Passed
Module Time:	0.0019509
Check CPU Real Time Clock	
Status:	Passed
Module Time:	6.6037957
Set Date	
Status:	Passed

End Sequence: CheckDiags

PowerVdd_SupplyStatus	
Status:	Passed
Module Time:	0.2877097
Measure_UUT_VddQuCurrent	

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Status:	Passed
Numeric:	0.069
Units:	A
Limits:	
Low:	0.03
High:	0.1
Comp:	GELE
Module Time:	0.8806573
DiagComTest	
Status:	Passed
Module Time:	0.3639637

End Sequence: UUTStartup

TestSerialOptions	
Status:	Passed
Module Time:	3.7400417

Begin Sequence: TestSerialOptions
(C:\GTS Files\Sequences\210000411\210000411.seq)

SerialOptionCPUWrt	
Status:	Passed
Module Time:	1.9228946
SerialOptCPUWrtSlot:0	
Status:	Passed
SerialOptCPUWrtSlot:1	
Status:	Passed
SerialOptCPUWrtSlot:2	
Status:	Passed
SerialOptCPUWrtSlot:3	
Status:	Passed
SerialOptionRead	
Status:	Passed
Module Time:	1.6319156
ColumnHeater300053 Degasser2005 AbsDegasser400a ColumnSwitcher500000a0	
SerialOptCPUReadCmdSlot:0	
Status:	Passed
SerialOptCPUReadCmdSlot:1	
Status:	Passed
SerialOptCPUReadCmdSlot:2	
Status:	Passed
SerialOptCPUReadCmdSlot:3	
Status:	Passed
SerialOptCPUReadMOSI_Slot:0	
Status:	Passed
SerialOptCPUReadMOSI_Slot:1	

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Status:	Passed
SerialOptCPUReadMOSI_Slot:2	
Status:	Passed
SerialOptCPUReadMOSI_Slot:3	
Status:	Passed

End Sequence: TestSerialOptions

TestOnboardVoltages	
Status:	Passed
Module Time:	11.2410946

Begin Sequence: TestOnboardVoltages
(C:\GTS Files\Sequences\210000411\210000411.seq)

Wait	
Status:	Done
Test 5VRef	
Status:	Passed
Numeric:	5.011
Units:	V
Limits:	
Low:	4.9
High:	5.1
Comp:	GELE
Module Time:	0.0760893
Wait	
Status:	Done
Wait	
Status:	Done
Test 3.3VPwr	
Status:	Passed
Numeric:	3.342
Units:	V
Limits:	
Low:	3.2
High:	3.5
Comp:	GELE
Module Time:	0.0762833
Wait	
Status:	Done
Test 2.5VPwr	
Status:	Passed
Numeric:	2.515
Units:	V
Limits:	
Low:	2.4
High:	2.7
Comp:	GELE

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Module Time:	0.0776892
Wait	
Status:	Done
Test 1.8VPwr	
Status:	Passed
Numeric:	1.805
Units:	V
Limits:	
Low:	1.75
High:	1.85
Comp:	GELE
Module Time:	0.0780637
Wait	
Status:	Done
Test Bat	
Status:	Passed
Numeric:	3.084
Units:	V
Limits:	
Low:	2.9
High:	3.5
Comp:	GELE
Module Time:	0.076269
TestAnalogOutput	
Status:	Done
TestAnalogOut	
Status:	Passed
Numeric:	0.01
Units:	V
Limits:	
Low:	-0.1
High:	0.1
Comp:	GELE
Module Time:	9.7192523

End Sequence: TestOnboardVoltages

TestCPUExpBus	
Status:	Passed
Module Time:	17.1750015

Begin Sequence: TestCPUExpBus
(C:\GTS Files\Sequences\210000411\210000411.seq)

Test ReadWrite Operations for Front Panel	
Status:	Done
TestFrontPanelReadVideoData	
Status:	Passed
Module Time:	1.8891109

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TestFrontPanelWriteVideoData	
Status:	Passed
Module Time:	1.2881619
TestFrontPanelReadKeyData	
Status:	Passed
Module Time:	1.8799137
TestFrontPanelWriteBackLightData	
Status:	Passed
Module Time:	0.3597225
TestFrontPanelWriteLCDPage	
Status:	Passed
Module Time:	0.9760421
TestFrontPanelReadIntpReg	
Status:	Passed
Module Time:	1.8829943
TestFrontPanelIntp	
Status:	Passed
Module Time:	0.5747683
Test ReadWrite Operations for Fluidics	
Status:	Done
TestFluidicsReadSensorReg1	
Status:	Passed
Module Time:	1.8856665
TestFluidicsReadSensorReg2	
Status:	Passed
Module Time:	1.6801383
TestFluidicsWriteMotorEnableReg	
Status:	Passed
Module Time:	1.4809759
TestFluidicsWriteMotorHoldReg	
Status:	Passed
Module Time:	1.4790139
TestFluidicsWriteMotorControlReg	
Status:	Passed
Module Time:	1.4787859

End Sequence: TestCPUExpBus

TestPressAcqu	
Status:	Passed
Module Time:	22.740904

Begin Sequence: TestPressAcqu
(C:\GTS Files\Sequences\210000411\210000411.seq)

TestPrimaryPressure	
Status:	Done
CheckPrimary Offset	
Status:	Passed

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Numeric:	41.22
Units:	psi
Limits:	
Low:	0
High:	60
Comp:	GELE
CheckPrimary psi/V	
Status:	Passed
Numeric:	2192.64
Units:	psi/V
Limits:	
Low:	2150
High:	2250
Comp:	GELE
TestPrimaryMidPressure	
Status:	Passed
Numeric:	-0.47
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.6580981
TestPrimaryHighPressure	
Status:	Passed
Numeric:	-0.67
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.6583947
TestSystemPressure	
Status:	Done
CheckSystem Offset	
Status:	Passed
Numeric:	41.9
Units:	psi
Limits:	
Low:	0
High:	60
Comp:	GELE
CheckSystem psi/V	
Status:	Passed
Numeric:	2193.05
Units:	psi/V
Limits:	

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Low:	2150
High:	2250
Comp:	GELE
TestSystemMidPressure	
Status:	Passed
Numeric:	-0.33
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.6570087
TestSystemHighPressure	
Status:	Passed
Numeric:	-0.93
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.6571712
TestSamplePressure	
Status:	Done
CheckSample Offset	
Status:	Passed
Numeric:	37.06
Units:	psi
Limits:	
Low:	0
High:	60
Comp:	GELE
CheckSample psi/V	
Status:	Passed
Numeric:	2193.06
Units:	psi/V
Limits:	
Low:	2150
High:	2250
Comp:	GELE
TestSampleMidPressure	
Status:	Passed
Numeric:	-0.47
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE

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Module Time:	0.6580072
TestSampleHighPressure	
Status:	Passed
Numeric:	-0.80
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.6579593
VerifyOvrPressEventsClr	
Status:	Passed
Module Time:	0.3648489
CheckPrimOvrPressEvent	
Status:	Passed
Module Time:	0.3648775
VerifyPrimOvrPressEventsClr	
Status:	Passed
Module Time:	0.3649237
CheckAccumOvrPressEvent	
Status:	Passed
Module Time:	0.3629632
VerifyAccumOvrPressEventsClr	
Status:	Passed
Module Time:	0.3650214

End Sequence: TestPressAcqu

TestPumpDrive	
Status:	Passed
Module Time:	53.8827431

Begin Sequence: TestPumpDrive
(C:\GTS Files\Sequences\210000411\210000411.seq)

Test Pump Drive	
Status:	Done
VerifyPumpEventsClr	
Status:	Passed
Module Time:	0.362687

MovePump	
Status:	Done
Module Time:	8.1159449
MovePump	
Status:	Done
Module Time:	8.1016448
MovePump	
Status:	Done
Module Time:	8.0606981

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MovePump	
Status:	Done
Module Time:	8.1028388

MotorPowerEnabled	
Status:	Passed
TestPrimaryPump	
Status:	Passed
TestAccumPump	
Status:	Passed
VerifyGPVFailClr	
Status:	Done
Module Time:	0.5047813
GPV Fail is Clr	
SetGPVStatusToFail	
Status:	Done
Module Time:	0.0030564
VerifyGPV_FailSet	
Status:	Done
Module Time:	0.5061402
GPV Fail is Set	
ClrGPVFail	
Status:	Done
Module Time:	0.3035559
VerifyGPV_FailClr	
Status:	Done
Module Time:	0.5063068
Test GPV Fail	
Status:	Passed
Test MTR Fail	
Status:	Done
VerifyMTR_FailClr	
Status:	Done
Module Time:	0.3656538
Motor Fail is Clr Acc Over Press is Clr Prim Over Press is Clr Prim Equall Press is Set	
VerifyMTR_FailSet	
Status:	Done
Module Time:	0.3648934
Motor Fail is Set Acc Over Press is Clr Prim Over Press is Clr Prim Equall Press is Set	
VerifyMTR_FailClr	
Status:	Done
Module Time:	0.8094488
Test MTR Fail	
Status:	Passed

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Motor Power Disabled	
Status:	Passed

End Sequence: TestPumpDrive

TestValveControl	
Status:	Passed
Module Time:	5.0583412

Begin Sequence: TestValveControl
(C:\GTS Files\Sequences\210000411\210000411.seq)

TestGPV-ValveControl	
Status:	Done
TestGPVContol_NONE	
Status:	Passed
Module Time:	0.3040837
TestGPVContol_A	
Status:	Passed
Module Time:	0.3031704
TestGPVContol_B	
Status:	Passed
Module Time:	0.3038372
TestGPVContol_C	
Status:	Passed
Module Time:	0.3030368
TestGPVContol_D	
Status:	Passed
Module Time:	0.3032913
TestSealWashValveControl	
Status:	Done
TestSealWashOff	
Status:	Passed
Module Time:	0.3033532
TestSealWashOn	
Status:	Passed
Module Time:	0.3030888
TestSpargeValveControl	
Status:	Done
TestSpargeAOff	
Status:	Passed
Module Time:	0.3033161
TestSpargeAOn	
Status:	Passed
Module Time:	0.3032743
TestSpargeBOff	
Status:	Passed
Module Time:	0.3031579
TestSpargeBOn	

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Status:	Passed
Module Time:	0.3032499
TestSpargeCOff	
Status:	Passed
Module Time:	0.3031814
TestSpargeCON	
Status:	Passed
Module Time:	0.3038355
TestSpargeDOff	
Status:	Passed
Module Time:	0.3031448
TestSpargeDON	
Status:	Passed
Module Time:	0.3051001

End Sequence: TestValveControl

TestEventsOut	
Status:	Passed
Module Time:	3.3216906

Begin Sequence: TestEventsOut
(C:\GTS Files\Sequences\210000411\210000411.seq)

TestEventsOut_Set0	
Status:	Passed
Module Time:	0.52702
TestEventsOut_Clr0	
Status:	Passed
TestEventsOut_Set1	
Status:	Passed
Module Time:	0.5257722
TestEventsOut_Clr1	
Status:	Passed
TestEventsOut_Set2	
Status:	Passed
Module Time:	0.5259712
TestEventsOut_Clr2	
Status:	Passed
TestEventsOut_Set3	
Status:	Passed
Module Time:	0.5265142
TestEventsOut_Clr3	
Status:	Passed
TestEventsOut_Set4	
Status:	Passed
Module Time:	0.5260165
TestEventsOut_Clr4	
Status:	Passed

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TestEventsOut_Set5	
Status:	Passed
Module Time:	0.5258815
TestEventsOut_Clr5	
Status:	Passed

End Sequence: TestEventsOut

TestFluidicDrive	
Status:	Passed
Module Time:	32.0076503

Begin Sequence: TestFluidicDrive
(C:\GTS Files\Sequences\210000411\210000411.seq)

V1Motor>>>	
Status:	Passed
Module Time:	0.3575895
V1Motor<<<	
Status:	Passed
Module Time:	0.3563069
V2Motor>>>	
Status:	Passed
Module Time:	0.3543513
V2Motor<<<	
Status:	Passed
Module Time:	0.3541636
zCarouselMotor>>>	
Status:	Passed
Module Time:	0.3545481
zCarouselMotor<<<	
Status:	Passed
Module Time:	0.3568373
DisMotor>>>	
Status:	Passed
Module Time:	0.4552562
DisMotor<<<	
Status:	Passed
Module Time:	0.458177
SyringeMotor>>>	
Status:	Passed
Module Time:	1.1591591
SyringeMotor<<<	
Status:	Passed
Module Time:	1.1790362
NeedleMotor>>>	
Status:	Passed
Module Time:	0.3056538
NeedleMotor<<<	

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Status:	Passed
Module Time:	0.3058642
xMotor>>>	
Status:	Passed
Module Time:	0.3035841
xMotor<<<	
Status:	Passed
Module Time:	0.3070647
yMotor>>>	
Status:	Passed
Module Time:	0.3066411
yMotor<<<	
Status:	Passed
Module Time:	0.3044258
zMotor>>>	
Status:	Passed
Module Time:	0.3046002
zMotor<<<	
Status:	Passed
Module Time:	0.3074966
RocketMotor>>>	
Status:	Passed
Module Time:	0.3038056
RocketMotor<<<	
Status:	Passed
Module Time:	0.3072972
CarrierMotor>>>	
Status:	Passed
Module Time:	0.4555203
CarouselMotor>>>	
Status:	Passed
Module Time:	0.3046276

MeasFluidic Clock	
Status:	Passed
Numeric:	10
Units:	MHz
Limits:	
Low:	9.99
High:	10.1
Comp:	GELE
Module Time:	0.0040818
Number of Loops:	1
Number of Passes:	1
Number of Failures:	0
Final Loop Index:	1

End Sequence: TestFluidicDrive

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TestPorts	
Status:	Passed
Module Time:	64.7287927

Begin Sequence: TestPorts
(C:\GTS Files\Sequences\210000411\210000411.seq)

TestRemotePort	
Status:	Passed
Module Time:	1.1673079

Ethernet Test	
Status:	Skipped

Ethernet Test	
Status:	Passed
Module Time:	4.2939971
CfgGPIBUUT_SlaveRecieve	
Status:	Done
Module Time:	2.9583762
GPIBUUT_SlaveRecieve	
Status:	Passed
Module Time:	2.210263
CfgGPIBUUT_SlaveReply	
Status:	Done
Module Time:	2.9643149
GPIBUUT_SlaveReply	
Status:	Passed
Module Time:	7.4328345
TestFloppyControl	
Status:	Passed
Module Time:	9.2922231

End Sequence: TestPorts

TestEventsIn	
Status:	Passed
Module Time:	9.7222062

Begin Sequence: TestEventsIn
(C:\GTS Files\Sequences\210000411\210000411.seq)

TestEventInActiveLow	
Status:	Done
InitPortActiveLow	
Status:	Done
Module Time:	0.369112
ActiveLow_0	
Status:	Passed
Module Time:	1.4702959
Set & Clr Passed	

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ActiveLow_1	
Status:	Passed
Module Time:	1.4739223
Set & Clr Passed	
ActiveLow_2	
Status:	Passed
Module Time:	1.468988
Set & Clr Passed	
TestEventInActiveHigh	
Status:	Done
InitPortActiveHigh	
Status:	Done
Module Time:	0.3665259
ActiveHigh_0	
Status:	Passed
Module Time:	1.4732192
Set & Clr Passed	
ActiveHigh_1	
Status:	Passed
Module Time:	1.4744884
Set & Clr Passed	
ActiveHigh_2	
Status:	Passed
Module Time:	1.4689108
Set & Clr Passed	

End Sequence: TestEventsIn

BeepLedReset	
Status:	Passed
Module Time:	39.8422529

Begin Sequence: BeepLedReset
(C:\GTS Files\Sequences\210000411\210000411.seq)

LED DS1 Test	
Status:	Passed
LED DS2 Test	
Status:	Passed
LED DS3 Test	
Status:	Passed
LED DS4 Test	
Status:	Passed
LED DS5 Test	
Status:	Passed
LED DS6 Test	
Status:	Passed
LED DS7 Test	
Status:	Passed

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LED DS8 Test	
Status:	Passed
Beeper Test	
Status:	Passed

End Sequence: BeepLedReset

End Sequence: MainSequence

End UUT Report

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Report No: TE0084031-EDV

Iteration No: 01

SAP No: TE0084031QA

Test name: Fault Insertion Test

Test Script No.: EDV-02

Equipment Number: TE0084031

Equipment Name: 2690 Alliance CPU Assembly Test Fixture

Software Version: 0.0

Part Number: 210000411

Serial Number: 150618132M

Purpose:

To verify that the equipment will fail a UUT that does not meet the critical to quality specifications under test.

Test execution:

Perform each of the fault insertion tests below. Record the actual result of the test, whether a fault was screened, and initial/date. After each Fault Insertion Method, reverse or remove the physical means of the failure before continuing with the next test.

Objective evidence:Completed Test Script Data Sheet
Screenshot of equipment software UI showing failure
Pictures of equipment pass/fail indicators, as applicable

Description	Fault Insertion Method	Expected Result	Actual Results	Fault Screened?	Initial & Date
1. UUT Startup		FAIL	Fail	yes	TJM 14 Jan 2019
1.1. CPU Reset Duration	Mask pin J26-23.	NaN	NAN	yes	TJM 14 Jan 2019
1.2. ExtSysResetDuration:		x = -1	-1	yes	miswak TJM 214 Jan 2019
1.3. PowerVcc_SupplyStatus	Short circuit the VCC1 and GND1 test points.	Fail	Fail	yes	TJM 14 Jan 2019
1.4. Measure_UUT_VccQuCurrent	Connect a 10 Ω resistor across the VCC1 and GND1 test points.	x > 0.8 V #35 A	1.112 A	yes	TJM 14 Jan 2019
1.5. Startup	Mask pin J8-2.	Fail	Fail	yes	TJM 14 Jan 2019
1.6. TE Firmware Installed		Fail	Fail	yes	TJM 14 Jan 2019
1.7. SerialOptStartupSlot:0	Mask pin J5-6.	Fail	Fail	yes	TJM 14 Jan 2019
1.8. SerialOptStartupSlot:1		Fail	Fail	yes	TJM 14 Jan 2019
1.9. SerialOptStartupSlot:2		Fail	Fail	yes	TJM 14 Jan 2019
1.10. SerialOptStartupSlot:3		Fail	Fail	yes	TJM 14 Jan 2019
1.11. CheckDiags		Fail	Fail	yes	TJM 14 Jan 2019
1.11.1. Check CPU Real Time Clock	Mask pin J5-4.	Fail	Fail	yes	TJM 14 Jan 2019
1.11.2. Set Date		Fail	Fail	yes	TJM 14 Jan 2019
1.12. PowerVdd_SupplyStatus	Short circuit the VDD1 and GND1 test points.	Fail	Fail	yes	TJM 14 Jan 2019

Report No: TE0084031-EDV

Iteration No: 01

SAP No: TE0084031QA

1.13. Measure_UUT_VddQuCurrent	Connect a 10 Ω resistor across the VDD1 and GND1 test points.	<i>TJM 22Jan2019 see deviation #35</i> $x > 0.1 \text{ A}$	<i>0.541 A</i>	<i>yes</i>	<i>TJM 14Jan2019</i>
2. TestSerialOptions		FAIL	Fail	yes	<i>TJM 14Jan2019</i>
2.1. SerialOptCPUWrtSlot: 0	Mask pin J5-4.	Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.2. SerialOptCPUWrtSlot: 1		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.3. SerialOptCPUWrtSlot: 2		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.4. SerialOptCPUWrtSlot: 3		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.5. SerialOptionRead		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.6. SerialOptCPUReadCmdSlot: 0		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.7. SerialOptCPUReadCmdSlot: 1		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.8. SerialOptCPUReadCmdSlot: 2		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.9. SerialOptCPUReadCmdSlot: 3		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.10. SerialOptCPUReadMOSI_Slot: 0		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.11. SerialOptCPUReadMOSI_Slot: 1		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.12. SerialOptCPUReadMOSI_Slot: 2		Fail	Fail	yes	<i>TJM 14Jan2019</i>
2.13. SerialOptCPUReadMOSI_Slot: 3		Fail	Fail	yes	<i>TJM 14Jan2019</i>
3. TestOnboardVoltages		FAIL	Fail	yes	<i>TJM 14Jan2019</i>
3.1. Test 5VRef	Mask the REF5V test point.	$x < 4.9 \text{ V}$	<i>0 V</i>	<i>yes</i>	<i>TJM 14Jan2019</i>
3.2. Test 3.3VPwr	Mask the 3.3V test point.	$x < 3.2 \text{ V}$	<i>0 V</i>	<i>yes</i>	<i>TJM 14Jan2019</i>
3.3. Test 2.5VPwr	Mask the 2.5V test point.	$x < 2.4 \text{ V}$	<i>0 V</i>	<i>yes</i>	<i>TJM 14Jan2019</i>
3.4. Test 1.8VPwr	Mask pin VR2.	$x < 1.75 \text{ V}$	<i>0 V</i>	<i>yes</i>	<i>TJM 14Jan2019</i>
3.5. TestBat	Mask pin BAT.	$x < 2.96 \text{ V}$	<i>0 V</i>	<i>yes</i>	<i>TJM 14Jan2019</i>
3.6. TestAnalogOut	Connect a 510 ohm resistor across J1-B11 and J1-B12 pins.	<i>TJM 22Jan2019 see deviation #4</i> $x > 0.1 \text{ V}$	<i>0.18 V</i>	<i>yes</i>	<i>TJM 14Jan2019</i>

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4. TestCPUExpBus		FAIL	Fail	yes	TJM 14 Jan 2019
4.1. TestFrontPanelReadVideoData	Mask pin J15-40.	Fail	Fail	yes	TJM 14 Jan 2019
4.2. TestFrontPanelWriteVideoData		Fail	Fail	yes	TJM 14 Jan 2019
4.3. TestFrontPanelReadKeyData		Fail	Fail	yes	TJM 14 Jan 2019
4.4. TestFrontPanelWriteBackLightData		Fail	Fail	yes	TJM 14 Jan 2019
4.5. TestFrontPanelWriteLCDPage		Fail	Fail	yes	TJM 14 Jan 2019
4.6. TestFrontPanelReadIntpReg		Fail	Fail	yes	TJM 14 Jan 2019
4.7. TestFrontPanelIntp		Fail	Fail	yes	TJM 14 Jan 2019
4.8. TestFluidicsReadSensorReg1		Fail	Fail	yes	TJM 14 Jan 2019
4.9. TestFluidicsReadSensorReg2		Fail	Fail	yes	TJM 14 Jan 2019
4.10. TestFluidicsWriteMotorEnableReg		Fail	Fail	yes	TJM 14 Jan 2019
4.11. TestFluidicsWriteMotorHoldReg		Fail	Fail	yes	TJM 14 Jan 2019
4.12. TestFluidicsWriteMotorControlReg		Fail	Fail	yes	TJM 14 Jan 2019
5. TestPressAcqu		FAIL	Fail	yes	TJM 16 Jan 2019
5.1. CheckPrimary Offset	Mask all the J20 pins.	x > 4000	8800 psi	yes	TJM 16 Jan 2019
5.2. CheckPrimary psi/V		x = 0	0 psi/v	yes	TJM 16 Jan 2019
5.3. TestPrimaryMidPressure		x = -3000	-3000 psi	yes	TJM 16 Jan 2019
5.4. TestPrimaryHighPressure		x = -6000	-6000 psi	yes	TJM 16 Jan 2019
5.5. CheckSystem Offset	Mask all the J21 pins.	x > 4000	8800 psi	yes	TJM 16 Jan 2019
5.6. CheckSystem psi/V		x < 2150	0 psi/v	yes	TJM 16 Jan 2019
5.7. TestSystemMidPressure		x = -3000	-3000 psi	yes	TJM 16 Jan 2019
5.8. TestSystemHighPressure		x = -6000	-6000 psi	yes	TJM 16 Jan 2019
5.9. CheckSample Offset	Mask all the J22 pins.	x > 4000	8800 psi	yes	TJM 16 Jan 2019
5.10. CheckSample psi/V		x < 2150	0 psi/v	yes	TJM 16 Jan 2019
5.11. CheckSampleMidPressure		x = -3000	-3000 psi	yes	TJM 16 Jan 2019
5.12. TestSampleHighPressure		x = -6000	-6000 psi	yes	TJM 16 Jan 2019
5.13. VerifyOvrPressEventsClr	Mask all the J20 pins.	Fail	Fail	yes	TJM 16 Jan 2019

5.14. CheckPrimOvrPressEvent	Connect a 300 Ω resistor across the J20-1 and J20-2 pins.	Fail	Fail	yes	TJM 16Jan2019
5.15. VerifyPrmOvrPressEventsClr	Mask all the J20 pins.	Fail	Fail	yes	TJM 16Jan2019
5.16. CheckAccumOvrPressEvent	Connect a 300 Ω resistor across the J21-1 and J21-2 pins.	Fail	Fail	yes	TJM 16Jan2019
5.17. VerifyAccumOvrPressEventsClr	Mask all the J21 pins.	Fail	Fail	yes	TJM 16Jan2019
6. TestPumpDrive		FAIL	Fail	yes	TJM 16Jan2019
6.1. VerifyPumpEventsClr	Mask all the J20 pins.	Fail	Fail	yes	TJM 16Jan2019
6.2. MotorPowerEnabled	Connect a 10 Ω resistor across the J26-22 pin and the GND1 test point.	Fail	Fail	yes	TJM 16Jan2019
6.3. TestPrimaryPump	Mask pin J23-6.	Fail	Fail	yes	TJM 16Jan2019
6.4. TestAccumPump	Mask pin J24-6.	Fail	Fail	yes	TJM 16Jan2019
6.5. Test GPV Fail	Mask pin J26-24.	Fail	Fail	yes	TJM 16Jan2019
6.6. Test MTR Fail	Insert a breakpoint at the "TestMTRFail" step. When the test reaches the breakpoint connect a 50 Ω resistor across the J26-25 pin and the VCC1 test point, then continue.	Fail	Fail	yes	TJM 16Jan2019
6.7. Motor Power Disabled	Connect a 50 Ω resistor across the J26-22 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16Jan2019
7. TestValveControl		FAIL	Fail	yes	TJM 16Jan2019
7.1. TestGPVControl_NONE	Connect a 50 Ω resistor across the J26-19 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16Jan2019
7.2. TestGPVControl_A		Fail	Fail	yes	TJM 16Jan2019
7.3. TestGPVControl_B		Fail	Fail	yes	TJM 16Jan2019
7.4. TestGPVControl_C		Fail	Fail	yes	TJM 16Jan2019
7.5. TestGPVControl_D	Mask J26-19.	Fail	Fail	yes	TJM 16Jan2019
7.6. TestSealWashOff	Connect a 50 Ω resistor across the J26-20 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16Jan2019

7.7. TestSealWashOn	Connect a 10 Ω resistor across the J26-20 pin and the GND1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.8. TestSpargeAOff	Connect a 10 Ω resistor across the J26-8 pin and the GND1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.9. TestSpargeAOn	Connect a 50 Ω resistor across the J26-8 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.10. TestSpargeBOff	Connect a 10 Ω resistor across the J26-10 pin and the GND1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.11. TestSpargeBOn	Connect a 50 Ω resistor across the J26-10 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.12. TestSpargeCOff	Connect a 10 Ω resistor across the J26-12 pin and the GND1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.13. TestSpargeCOn	Connect a 50 Ω resistor across the J26-12 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.14. TestSpargeDOff	Connect a 10 Ω resistor across the J26-15 pin and the GND1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
7.15. TestSpargeDOn	Connect a 50 Ω across the J26-15 pin and the VCC1 test point.	Fail	Fail	yes	TJM 16 Jan 2019
8. TestEventsOut		FAIL	Fail	yes	TJM 16 Jan 2019
8.1. TestEventsOut_Set0	Short circuit pins J1-A1 and J1-A2.	Fail	Fail	yes	TJM 16 Jan 2019
8.2. TestEventsOut_Clr0	Mask pin J1-A2.	Fail	Fail	yes	TJM 16 Jan 2019
8.3. TestEventsOut_Set1	Short circuit pins J1-A4 and J1-A5.	Fail	Fail	yes	TJM 16 Jan 2019
8.4. TestEventsOut_Clr1	Mask pin J1-A5.	Fail	Fail	yes	TJM 16 Jan 2019
8.5. TestEventsOut_Set2	Short circuit pins J1-A6 and J1-A7.	Fail	Fail	yes	TJM 16 Jan 2019
8.6. TestEventsOut_Clr2	Mask pin J1-A7.	Fail	Fail	yes	TJM 16 Jan 2019
8.7. TestEventsOut_Set3	Short circuit pins J1-A8 and J1-A9.	Fail	Fail	yes	TJM 16 Jan 2019
8.8. TestEventsOut_Clr3	Mask pin J1-A9.	Fail	Fail	yes	TJM 16 Jan 2019

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8.9. TestEventsOut_Set4	Short circuit pins J1-A11 and J1-A12.	Fail	Fail	yes	TJM 16 Jan 2019
8.10. TestEventsOut_Clr4	Mask pin J1-A12.	Fail	Fail	yes	TJM 16 Jan 2019
8.11. TestEventsOut_Set5	Short circuit pins J1-B1 and J1-B2.	Fail	Fail	yes	TJM 16 Jan 2019
8.12. TestEventsOut_Clr5	Mask pin J1-B2.	Fail	Fail	yes	TJM 16 Jan 2019
9. TestFluidicDrive		FAIL	Fail	yes	TJM 17 Jan 2019
9.1. V1Motor>>>	Mask pin J25-36.	Fail	Fail	yes	TJM 17 Jan 2019
9.2. V1Motor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.3. V2Motor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.4. V2Motor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.5. ZCarouselMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.6. ZCarouselMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.7. DisMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.8. DisMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.9. SyringeMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.10. SyringeMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.11. NeedleMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.12. NeedleMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.13. XMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.14. XMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.15. YMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.16. YMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.17. ZMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.18. ZMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.19. RocketMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.20. RocketMotor<<<		Fail	Fail	yes	TJM 17 Jan 2019
9.21. CarrierMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019
9.22. CarouselMotor>>>		Fail	Fail	yes	TJM 17 Jan 2019

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9.23. MeasFluidicClock	Mask pin J25-24.	NaN	NaN	yes	TJM 17Jan2019
10. TestPorts		FAIL	Fail	yes	TJM 17Jan2019
10.1. TestRemotePort	Connect a 50 Ω resistor across the RS232-2 pin and GND1 test point.	Fail	Fail	yes	TJM 17Jan2019
10.2. Ethernet Test	Disconnect the ethernet cable from the fixture and select that the cable is plugged in when prompted by the test program.	Fail	Fail	yes	TJM 17Jan2019
10.3. GPIBUUT_SlaveRecieve	Mask pin J16-1.	Fail	Fail	yes	TJM 17Jan2019
10.4. GPIBUUT_SlaveReply		Fail	Fail	yes	TJM 17Jan2019
10.5. TestFloppyControl	Mask pin J27-5.	Fail	Fail	yes	TJM 17Jan2019
11. TestEventsIn		FAIL	Fail	yes	TJM 17Jan2019
11.1. ActiveLow_0	Connect a 50 Ω across the J1-B4 pin and the VCC1 test point.	Fail	Fail	yes	TJM 17Jan2019
11.2. ActiveLow_1	Connect a 50 Ω resistor across the J1-B6 pin and the VCC1 test point.	Fail	Fail	yes	TJM 17Jan2019
11.3. ActiveLow_2	Connect a 50 Ω across the J1-B8 pin and the VCC test point.	Fail	Fail	yes	TJM 17Jan2019
11.4. ActiveHigh_0	Connect a 50 Ω across the J1-B4 pin and the GND test point.	Fail	Fail	yes	TJM 17Jan2019
11.5. ActiveHigh_1	Connect a 50 Ω resistor across the J1-B6 pin and the GND test point.	Fail	Fail	yes	TJM 17Jan2019
11.6. ActiveHigh_2	Connect a 50 Ω resistor across the J1-B8 pin and the GND test point.	Fail	Fail	yes	TJM 17Jan2019

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12. BeepLedReset		FAIL	Fail	yes	TJM 17Jan2019
12.1. LED DS1 Test	Select that each light is not illuminated when prompted by the test program.	Fail	Fail	yes	TJM 17Jan2019
12.2. LED DS2 Test		Fail	Fail	yes	TJM 17Jan2019
12.3. LED DS3 Test <i>protocol typo.</i>		Fail	Fail	yes	TJM 17Jan2019
12.4. LED DS4 ^{DS4} Test <i>TJM 17Jan2019 *</i>		Fail	Fail	yes	TJM 17Jan2019
12.5. LED DS5 Test		Fail	Fail	yes	TJM 17Jan2019
12.6. LED DS6 Test		Fail	Fail	yes	TJM 17Jan2019
12.7. LED DS7 Test		Fail	Fail	yes	TJM 17Jan2019
12.8. LED DS8 Test		Fail	Fail	yes	TJM 17Jan2019
12.9. Beeper Test	Select that the beeper was not on when prompted by the test program.	Fail	Fail	yes	TJM 17Jan2019

Comments:

* see deviation #2 for explanation of this protocol issue. *TJM 17Jan2019*

** see deviation #3 for explanation of this protocol issue. *TJM 17Jan2019*

There were also deviations in steps 1.4 ? 1.13 in EDV-02. *TJM 17Jan2019*

see deviation #5 for explanation. *TJM 22Jan2018*
2019 TJM 22Jan2019

There was also a deviation in step 3.5 in EDV-02. *TJM 22Jan2019*

see deviation #4 for explanation. *TJM 22Jan2019*

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Overall Test Conclusion:

☒ Fail

Pass

☐ Fail

Step 1.1

CPU Reset Duration	
Status:	Failed
Numeric:	NAN
Units:	ms
Limits:	
Low:	3.30
High:	4.00
Comp:	GELE

Step 1.2

ExtSysResetDuration	
Status:	Failed
Numeric:	1.00
Units:	ms
Limits:	
Low:	0.30
High:	0.70
Comp:	GELE

Step 1.3

PowerVcc_SupplyStatus	
Status:	Failed
Module Time:	0.0506411

Step 1.4

Measure_UUT_VccQuCurrent	
Status:	Failed
Numeric:	1.112
Units:	A
Limits:	
Low:	0.3
High:	0.8
Comp:	GELE
Module Time:	0.6106

Step 1.5

Startup	
Status:	Failed
Module Time:	50.2095728

Step 1.6

TE Firmware Installed	
Status:	Failed

Step 1.7

SerialOptStartupSlot:0	
Status:	Failed

Step 1.8

SerialOptStartupSlot:1	
Status:	Failed

Step 1.9

SerialOptStartupSlot:2	
Status:	Failed

Step 1.10

SerialOptStartupSlot:3	
Status:	Failed

Step 1.11

CheckDiags	
Status:	Failed
Module Time:	0.1262211

Step 1.11.1

Check CPU Real Time Clock	
Status:	Error
Error Message: Scan From String (arg 1) in CheckRealTimeClock or xCheckRealTimeClock in ProxyCalatariVIEW: Scan failed. The next string does not contain data in the expected format. (Error Code: 85)	
Module Time:	5.3719033

Step 1.11.2

Set Date	
Status:	Failed

Step 1.12

PowerVdd_SupplyStatus	
Status:	Failed
Module Time:	0.2751431

Step 1.13

Measure_UUT_VddOuCurrent	
Status:	Failed
Numeric:	0.541
Units:	A
Limits:	
Low:	0.03
High:	0.1
Comp:	GELE
Module Time:	0.8611493

Step 2.1

SerialOptCPUWrtSlot:0	
Status:	Failed

Step 2.2

SerialOptCPUWrtSlot:1	
Status:	Failed

Step 2.3

SerialOptCPUWrtSlot:2	
Status:	Failed

Step 2.4

SerialOptCPUWrtSlot:3	
Status:	Failed

Step 2.5

SerialOptionRead	
Status:	Failed
Module Time:	0.026088

Step 2.6

SerialOptCPUReadCmdSlot:0	
Status:	Failed

Step 2.7

SerialOptCPUReadCmdSlot:1	
Status:	Failed

Step 2.8

SerialOptCPUReadCmdSlot:2	
Status:	Failed

Step 2.9

SerialOptCPUReadCmdSlot:3	
Status:	Failed

Step 2.10

SerialOptCPUReadMOSI_Slot:0	
Status:	Failed

Step 2.11

SerialOptCPUReadMOSI_Slot:1	
Status:	Failed

Step 2.12

SerialOptCPUReadMOSI_Slot:2	
Status:	Failed

Step 2.13

SerialOptCPUReadMOSI_Slot:3	
Status:	Failed

Step 3.1

Test 5VRef	
Status:	Failed
Numeric:	0
Units:	V
Limits:	
Low:	4.9
High:	5.1
Comp:	GELE
Module Time:	0.0869679

Step 3.2

Test 3.3VPwr	
Status:	Failed
Numeric:	0
Units:	V
Limits:	
Low:	3.2
High:	3.5
Comp:	GELE
Module Time:	0.0955087

Step 3.3

Test 2.5VPwr	
Status:	Failed
Numeric:	0
Units:	V
Limits:	
Low:	2.4
High:	2.7
Comp:	GELE
Module Time:	0.0784568

Step 3.4

Test 1.8VPwr	
Status:	Failed
Numeric:	0
Units:	V
Limits:	
Low:	1.75
High:	1.85
Comp:	GELE
Module Time:	0.0798132

Step 3.5

Test Bat	
Status:	Failed
Numeric:	0
Units:	V
Limits:	
Low:	2.9
High:	3.5
Comp:	GELE
Module Time:	0.1024352

Step 3.6

TestAnalogOut	
Status:	Failed
Numeric:	0.18
Units:	V
Limits:	
Low:	-0.1
High:	0.1
Comp:	GELE
Module Time:	9.7409758

Step 4.1

TestFrontPanelReadVideoData	
Status:	Failed

Step 4.2

TestFrontPanelWriteVideoData	
Status:	Failed

Step 4.3

TestFrontPanelReadKeyData	
Status:	Failed

Step 4.4

TestFrontPanelWriteBackLightData	
Status:	Failed

Step 4.5

TestFrontPanelWriteLCDPage	
Status:	Failed

Step 4.6

TestFrontPanelReadIntpReg	
Status:	Failed

Step 4.7

TestFrontPanelIntp	
Status:	Failed

Step 4.8

TestFluidicsReadSensorReg1	
Status:	Failed

Step 4.9

TestFluidicsReadSensorReg2	
Status:	Failed

Step 4.10

TestFluidicsWriteMotorEnableReg	
Status:	Failed

Step 4.11

TestFluidicsWriteMotorHoldReg	
Status:	Failed

Step 4.12

TestFluidicsWriteMotorControlReg	
Status:	Failed

Step 5.1

CheckPrimary Offset	
Status:	Failed
Numeric:	8800
Units:	psi
Limits:	
Low:	0
High:	60
Comp:	SELE

Step 5.2

CheckPrimary psi/V	
Status:	Failed
Numeric:	0
Units:	psi/V
Limits:	
Low:	2150
High:	2250
Comp:	SELE

Step 5.3

TestPrimaryMidPressure	
Status:	Failed
Numeric:	-3000.00
Units:	psi
Limits:	
Low:	10.00
High:	10.00
Comp:	GELE
Module Time:	0.0312625

Step 5.4

TestPrimaryHighPressure	
Status:	Failed
Numeric:	-6000.00
Units:	psi
Limits:	
Low:	10.00
High:	10.00
Comp:	GELE
Module Time:	0.0026374

Step 5.5

CheckSystem Offset	
Status:	Failed
Numeric:	8800
Units:	psi
Limits:	
Low:	0
High:	60
Comp:	GELE

Step 5.6

CheckSystem psi/V	
Status:	Failed
Numeric:	0
Units:	psi/V
Limits:	
Low:	2150
High:	2250
Comp:	GELE

Step 5.7

TestSystemMidPressure	
Status:	Failed
Numeric:	-3000.00
Units:	psi
Limits:	
Low:	10.00
High:	10.00
Comp:	GELE
Module Time:	0.0028377

Step 5.8

TestSystemHighPressure	
Status:	Failed
Numeric:	-6000.00
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.0025456

Step 5.9

CheckSample Offset	
Status:	Failed
Numeric:	6600
Units:	psi
Limits:	
Low:	0
High:	60
Comp:	GELE

Step 5.10

CheckSample psi/V	
Status:	Failed
Numeric:	0
Units:	psi/V
Limits:	
Low:	2150
High:	2250
Comp:	GELE

Step 5.11

TestSampleMidPressure	
Status:	Failed
Numeric:	-1000.00
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.0029809

Step 5.12

TestSampleHighPressure	
Status:	Failed
Numeric:	-5000.00
Units:	psi
Limits:	
Low:	-10.00
High:	10.00
Comp:	GELE
Module Time:	0.0033428

Step 5.13

VerifyOvrPressEventsClr	
Status:	Failed

Step 5.14

CheckPrimOvrPressEvent	
Status:	Failed
Module Time:	0.3608562

Step 5.15

VerifyPrimOvrPressEventCir	
Status:	Failed

Step 5.16

CheckAccumOvrPressEvent	
Status:	Failed

Step 5.17

VerifyAccumOvrPressEventCir	
Status:	Failed

Step 6.1

VerifyPumpEventsCir	
Status:	Failed

Step 6.2

MotorPowerEnabled	
Status:	Failed

Step 6.3

TestPrimaryPump	
Status:	Failed

Step 6.4

TestAccumPump	
Status:	Failed

Step 6.5

Test GPV Fail	
Status:	Failed

Step 6.6

Test MTR Fail	
Status:	Failed

Step 6.7

Motor Power Disabled	
Status:	Failed

Step 7.1

TestGPVControl_NONE	
Status:	Failed

Step 7.2

TestGPVControl_A	
Status:	Failed

Step 7.3

TestGPVContol_B	
Status:	Failed

Step 7.4

TestGPVContol_C	
Status:	Failed

Step 7.5

TestGPVContol_D	
Status:	Failed

Step 7.6

TestSealWashOff	
Status:	Failed

Step 7.7

TestSealWashOn	
Status:	Failed

Step 7.8

TestSpargeAOff	
Status:	Failed

Step 7.9

TestSpargeAOn	
Status:	Failed

Step 7.10

TestSpargeBOff	
Status:	Failed

Step 7.11

TestSpargeBOn	
Status:	Failed

Step 7.12

TestSpargeCOff	
Status:	Failed

Step 7.13

TestSpargeCOn	
Status:	Failed

Step 7.14

TestSpargeDOff	
Status:	Failed

Step 7.15

TestSpargeDOn	
Status:	Failed

Step 8.1

TestEventsOut_Set0
Status:
Failed

Step 8.2

TestEventsOut_Clr0
Status:
Failed

Step 8.3

TestEventsOut_Set1
Status:
Failed

Step 8.4

TestEventsOut_Clr1
Status:
Failed

Step 8.5

TestEventsOut_Set2
Status:
Failed

Step 8.6

TestEventsOut_Clr2
Status:
Failed

Step 8.7

TestEventsOut_Set3
Status:
Failed

Step 8.8

TestEventsOut_Clr3
Status:
Failed

Step 8.9

TestEventsOut_Set4
Status:
Failed

Step 8.10

TestEventsOut_Clr4
Status:
Failed

Step 8.11

TestEventsOut_Set5
Status:
Failed

Step 8.12

TestEventsOut_Clr5
Status:
Failed

Step 9.1

VI Motor>>>
Status:
Failed

Step 9.2

V1Motor<<<	
Status:	Fail

Step 9.3

V2Motor>>>	
Status:	Fail

Step 9.4

V2Motor<<<	
Status:	Fail

Step 9.5

zCarouselMotor>>>	
Status:	Fail

Step 9.6

zCarouselMotor<<<	
Status:	Fail

Step 9.7

DisMotor>>>	
Status:	Fail

Step 9.8

DisMotor<<<	
Status:	Fail

Step 9.9

SyringeMotor>>>	
Status:	Fail

Step 9.10

SyringeMotor<<<	
Status:	Fail

Step 9.11

NeedleMotor>>>	
Status:	Fail

Step 9.12

NeedleMotor<<<	
Status:	Fail

Step 9.13

xMotor>>>	
Status:	Fail

Step 9.14

xMotor<<<	
Status:	Fail

Step 9.15

yMotor>>>	
Status:	Failed

Step 9.16

yMotor<<<	
Status:	Failed

Step 9.17

zMotor>>>	
Status:	Failed

Step 9.18

zMotor<<<	
Status:	Failed

Step 9.19

RocketMotor>>>	
Status:	Failed

Step 9.20

RocketMotor<<<	
Status:	Failed

Step 9.21

CarrierMotor>>>	
Status:	Failed

Step 9.22

CarouselMotor>>>	
Status:	Failed

Step 9.23

MeasFluidic Clock	
Status:	Failed
Numeric:	NAN
Units:	MHz
Limits:	
Low:	9.99
High:	10.1
Comp:	GELE
Module Time:	30.0204061
Number of Loops:	3
Number of Passes:	0
Number of Failures:	3
Final Loop Index:	3

Step 10.1

TestRemotePort	
Status:	Failed

Step 10.2

Ethernet Test	
Status:	Failed

Step 10.3

GPIBUUT_SlaveRecieve	
Status:	Failed

Step 10.4

GPIBUUT_SlaveReply	
Status:	Failed

Step 10.5

TestFloppyControl	
Status:	Failed

Step 11.1

ActiveLow_0	
Status:	Failed

Step 11.2

ActiveLow_1	
Status:	Failed

Step 11.3

ActiveLow_2	
Status:	Failed

Step 11.4

ActiveHigh_0	
Status:	Failed

Step 11.5

ActiveHigh_1	
Status:	Failed

Step 11.6

ActiveHigh_2	
Status:	Failed

Step 12.1

LED_DS1_Test	
Status:	Failed

Step 12.2

LED_DS2_Test	
Status:	Failed

Step 12.3

LED_DS3_Test	
Status:	Failed

Step 12.4

LED_DS4_Test	
Status:	Failed

Step 12.5

LED_DS5_Test	
Status:	Failed

Step 12.6

LED DS6 Test	
Status:	Failed

Step 12.7

LED DS7 Test	
Status:	Failed

Step 12.8

LED DS8 Test	
Status:	Failed

Step 12.9

Beeper Test	
Status:	Failed

Screenshot of test software showing software version:

